INSTALLATION AND SERVICE
MANUAL

MODEL 2644A
MINI DATA STATION

Manual part no. 02644-90002
Microfiche part no. 02644-90003

Printed: OCT 1975

HEWLETT hp PACKARD

LIST OF EFFECTIVE PAGES

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OPTIONS COVERED

This manual covers options 001, 008, 012, and 015 as well as the standard model terminal.

ACCESSORIES COVERED

This manual covers the following terminal accessories:

13231A Display Enhancements
13231A-201 Mathematic Set
13231A-202 Line Drawing Set
13232A 103/202 Modem Cable Assembly
13232B 12531/12880 Interface Cable Assembly
13232C RS232C Cable Assembly
13236A Cartridge Tape
13238A Terminal Duplex Register
13238A-001 HP 9866 Cable Assembly
13245A Character Set Generation Kit
13246A Printer Subsystem (9866)

HEWLETT-PACKARD COMPANY
11000 WOLFE ROAD, CUPERTINO, CALIFORNIA, U.S.A.

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PREFACE

This manual provides field service instructions for the Hewlett-Packard 2644A MiniData Station; a CRT display terminal with mass storage capabilities. The HP 2644A is a state-of-the art product and, because of product design, a complete modular philosophy has been implemented to minimize on-site time for installing add-on accessories and for repair. Initial installation instructions and user preventive maintenance procedures for the terminal are contained in the *HP 2644A MiniData Station Owner's Manual,* part no. 02644-90001.

CONTENTS

ILLUSTRATIONS

TABLES

INSTALLATION

SECTION I

1-1. INTRODUCTION

This section contains instructions for selecting optional ac operating voltages (115 or 230V), selecting optional operating functions, instructions for installing mini data station (terminal) add-on accessories, and instructions for unpacking and repackaging the terminal.

WARNING

Hazardous voltages are present inside equipment. The procedures contained in this section shall be performed only by qualified service personnel.

VORSICHT

Innerhalb des Geräts bestehen gefährliche Spannungen. Die in diesem Abschnitt enthaltenen Arbeiten dürfen nur durch Betriebsfachpersonal durchgeführt werden.

ATTENTION

Des tensions dangereuses sont présentes à l'intérieur du matériel. Les opérations décrites dans cette section ne devront être effectuées que par un personnel qualifié.

AVVISO

Pericolo: Alta tensione presente in questa apparecchiatura. Le procedure contenute in questa sezione debbono essere effettuate soltanto da qualificato personale di servizio.

ADVERTENCIA

Hay voltaje peligroso en el interior de este equipo. Los procedimientos expuestos en esta sección sólo deberá llevarlos a cabo el personal de servicio calificado.

高圧危険

内部装置に危険な高電圧がきています　この章にある処置や手続に関しては、専門のサービスマンによってのみ行なって下さい

1-2. OPENING THE TERMINAL

To gain access to the terminal internal components, open the terminal as follows:

a. Set mainframe rear panel AC POWER switch to OFF and disconnect power cord from LINE connector.

Note: Mainframe top cover is unlocked by inserting access key supplied with terminal in each of the keyways located on right and left sides of top cover. Inserting keys into keyways unlock top cover. No key rotation is required.

b. From front of terminal, insert access key into right keyway and unlock right side of terminal by slightly raising right side of top cover.

c. While maintaining upward pressure to keep right side of terminal unlocked, insert access key into left keyway and raise top cover until both right and left sides of terminal are unlocked.

d. Using both hands, carefully swing top cover up until it latches into the half open position.

Note: The half open position provides adequate room for performing most service routines. However, if extensive repairs are to be made or if components contained in the top cover are to be serviced, fully open mainframe in accordance with step d.

CAUTION

Mainframe top hinges are open hinge type. When fully opening terminals do not allow top hinges to slip off hinge pins.

e. Firmly grasp top cover in one hand and release safety latch (see figure 1-1) by pressing it inboard with other hand. Then, using both hands, swing top cover up and over to a full open position (resting on its top).

1-3. ACCESSORY INSTALLATION PROCEDURES

Instructions for installing add-on accessories to the standard model terminal are contained in paragraphs 1-4 through 1-9.

Note: After installing any accessory, always use the terminal self-test feature (Section III) to ensure proper operation.

1-4. HP 13238A TERMINAL DUPLEX REGISTER

These instructions apply to both the HP 13238A and HP 13238A-001 add-on accessories. To install the HP 13238A accessory, perform all the following steps except steps d and e. To install the HP 13238A-001 accessory, perform all the following steps.

a. Open terminal to its half open position in accordance with paragraph 1-2.

b. Configure jumpers in Terminal Duplex Register PCA jumper sockets as shown in figure 1-3.

c. Install Terminal Duplex Register PCA in first vacant Backplane Assembly connector adjacent to existing PCA's.

Note: To ensure proper terminal operation, all PCA's must be installed in adjacent Backplane Assembly connectors. There should never be vacant connectors between PCA's except for the two CTU PCA's (Read/Write PCA and CTU Interface PCA) which can be separated from the others.

CAUTION

Do not attempt to force hood connector on PCA connector. Failure to comply may result in damage to both the hood connector and PCA.

d. Open mainframe rear door by twisting two lock extrusions.

e. Holding Terminal Duplex Register PCA firmly in place, carefully connect hood connector of HP 9866 Cable Assembly, part no. 13238-60001, to PCA connector P2.

Note: The hood connector and PCA connector P2 are identically keyed to prevent inadvertant erroneous connections. Connecting the two together requires minimal hand pressure. If excessive resistance is encountered, an incorrect connection is being attempted.

Note: For printer interfacing information refer to the *HP 9866A Printer Service Manual*, part no. 09866-90030.

f. Check and, if necessary, adjust power supply in accordance with paragraph 3-10.

g. Firmly grasp mainframe top cover in one hand and release safety latch by pressing it inboard with other hand. Then, using both hands, carefully lower top cover to its closed position.

1-5. HP 13246A PRINTER SUBSYSTEM (9866)

This accessory consists of a Terminal Duplex Register PCA, part no. 02640-60031; a 9866 Cable Assembly, part no. 13238-60031; and an HP 9866A Printer. To install this accessory, first perform the installation instructions contained in paragraph 1-4, steps a through g. After the PCA and cable assembly have been installed, install the printer in accordance with the instructions contained in the HP 9866A *Printer Peripheral Manual*, part no. 09866-90000 and the HP 9866A *Printer Service Manual*, part no. 09866-90030.

1-6. HP 13231A DISPLAY ENHANCEMENTS

These instructions apply to the HP 13231A-201 and HP 13231A-202 accessories as well as the HP 13231A accessory. The HP 13231A accessory consists of a Display Expansion PCA, part no. 02640-60024; a Top Plane Connector Assembly, part no. 02640-60022; and a Connector Removal Tool, part no. 02640-00029. The HP 13231A-201 and -202 accessories consist of the same three items with the applicable ROM IC's mounted on the Display Expansion PCA. Install any of these accessories as follows:

a. Using figure 1-4 and table 1-1 as a guide, check that Display Expansion PCA jumpers are arranged correctly for the ROM character set configuration. If there are no alternate character set ROM's installed (HP 13231A), all jumpers should be in the jumper socket.

b. Open terminal to its half open position in accordance with paragraph 1-2.

c. Insert connector removal tool under Top Plane Assembly as shown in figure 1-5.

d. Remove Top Plane Assembly by pressing down on connector removal tool handle. Retain Top Plane Assembly for possible future use.

e. If necessary, rearrange PCAs in Backplane Assembly so that an unused connector is available for the Display Expansion PCA adjacent to the Display Memory Access (DMA), Display Control, and Display Timing PCA's.

Note: PCA arrangement can be in any configuration with the following exceptions. The Keyboard Interface PCA should be installed in one of the first five Backplane Assembly connectors closest to the power supply. The Display Expansion, DMA, Display Control, and Display Timing PCA's must always be installed as a group in adjacent connectors. The CTU Interface and Read/Write PCA's must always be

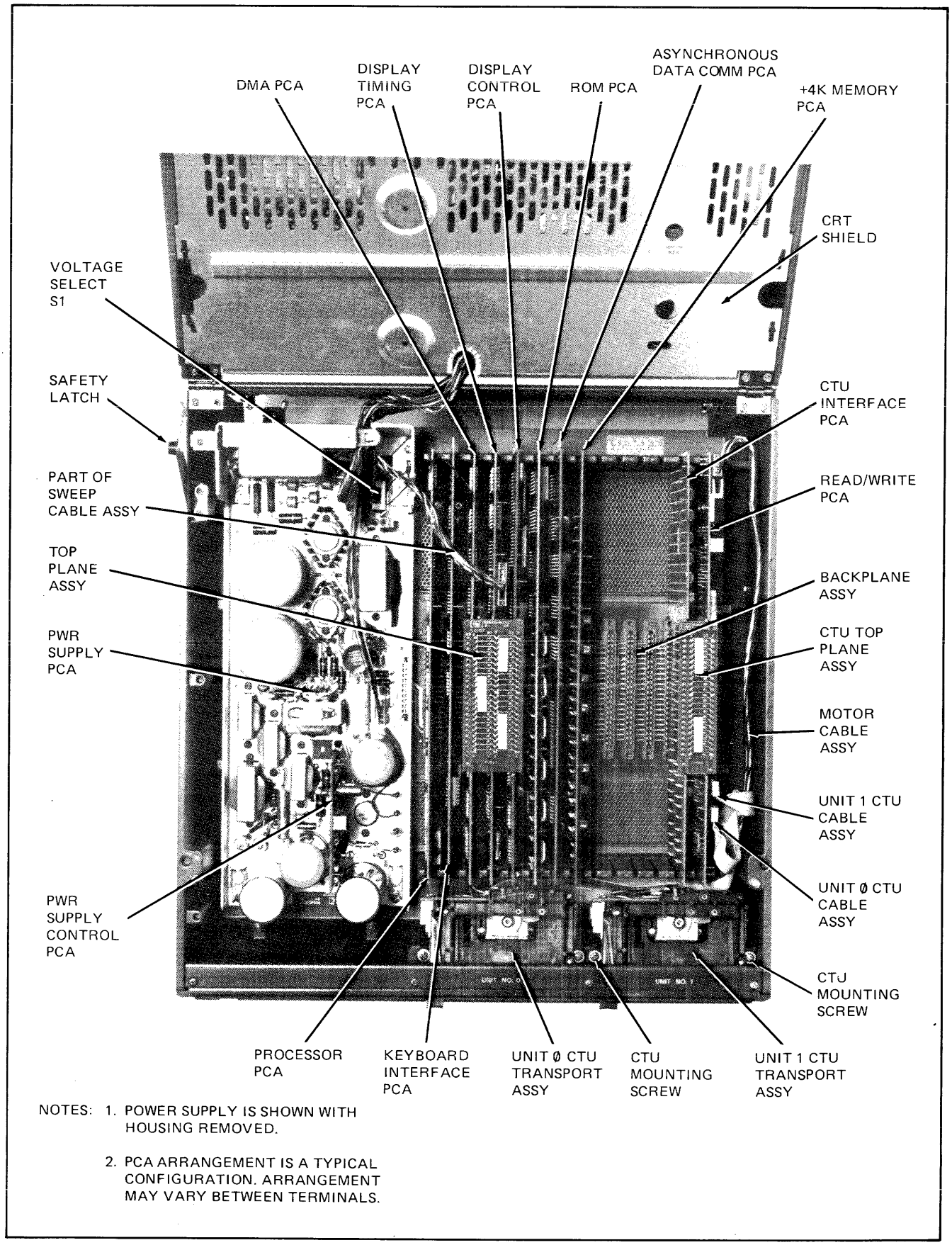

Figure 1-1. Mainframe Bottom Part Locations

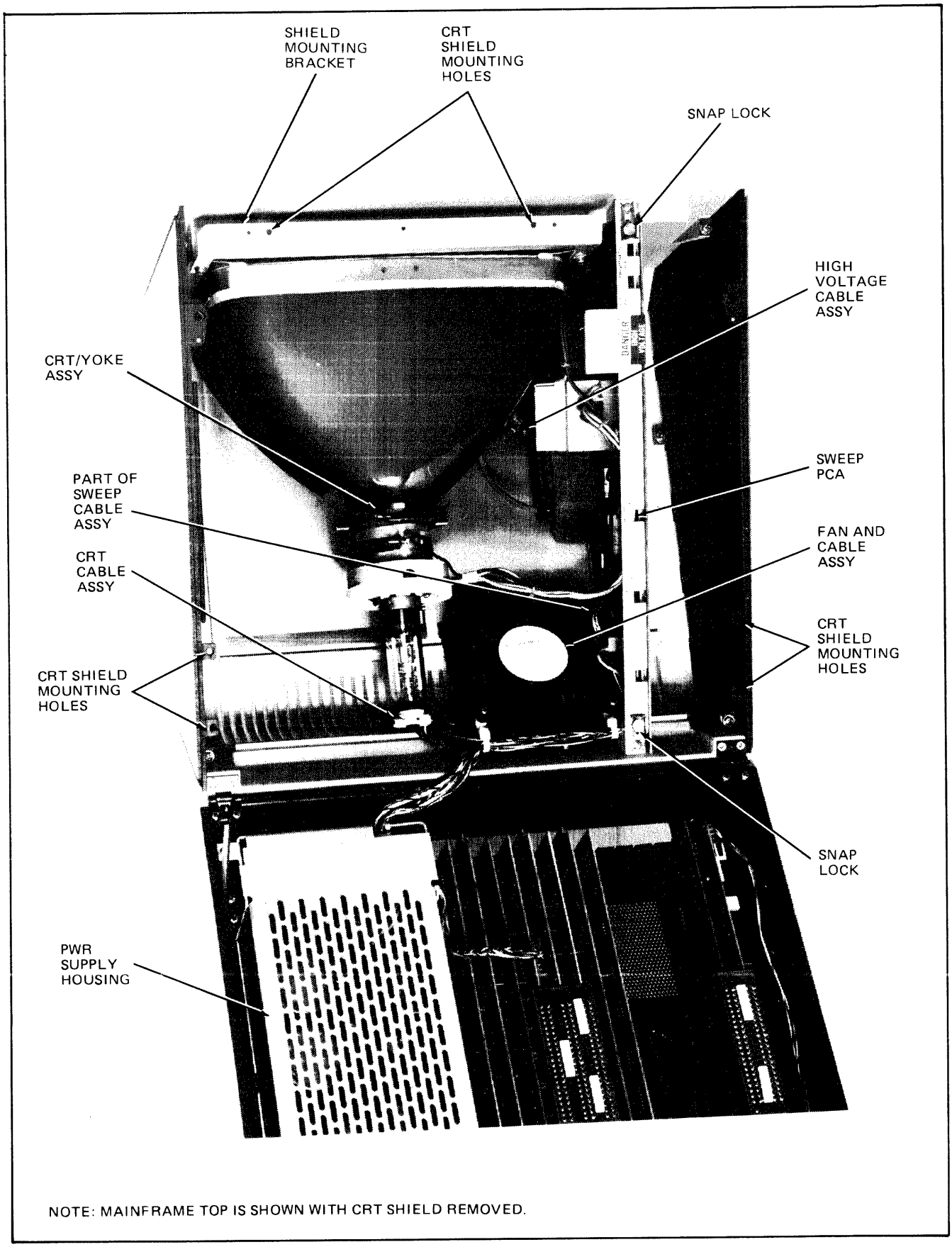

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Figure 1-2. Mainframe Top Part Locations

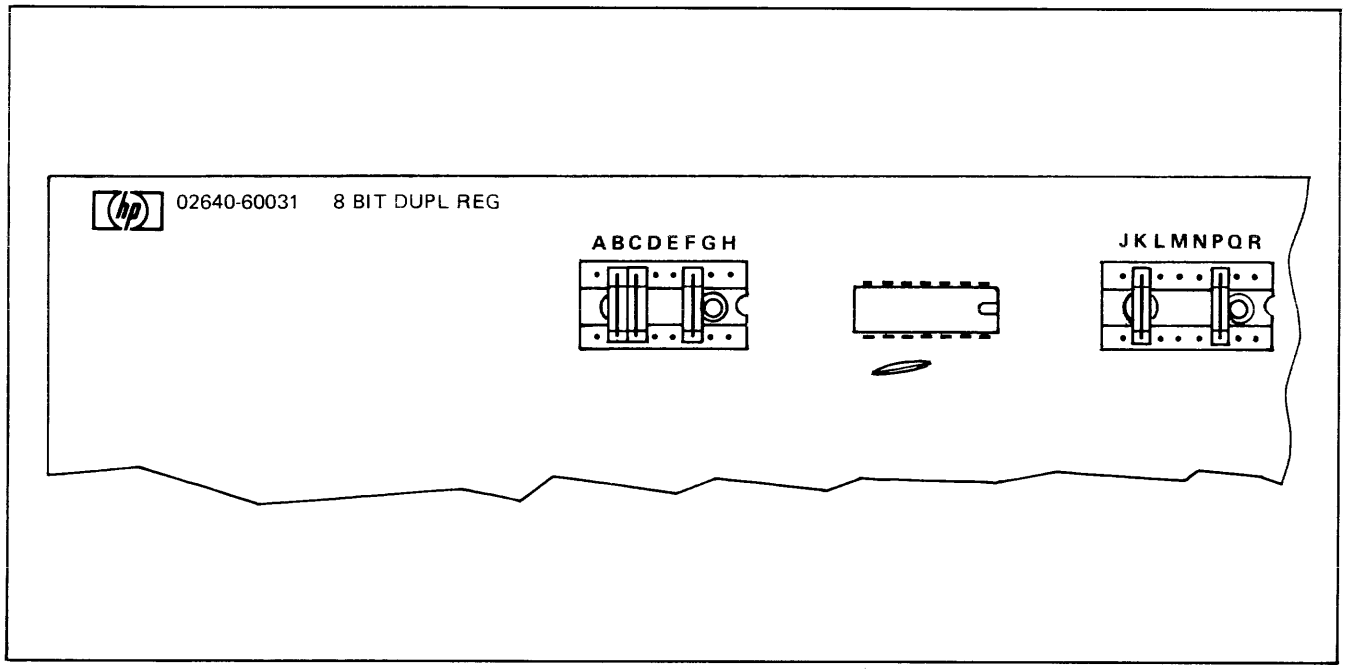

Figure 1-3. Terminal Duplex Register PCA Jumper Configuration

Table 1-1. Display Expansion PCA Jumper Protocol

SET NO.	JUMPER NO.	128 CHARACTERS (64 Upper Case and 64 Lower Case)	64 CHARACTERS (64 Upper Case)	MATH SET (Alphanumeric)	LINE SET (Microvector)
1	1	IN	OUT		
	2			IN	OUT
2	3	IN	OUT		
	4			IN	OUT
3	5	IN	OUT		
	6			IN	OUT

installed in adjacent connectors. No Backplane Assembly connectors can be left vacant between any PCA's except for the two CTU PCA's which can be separated from the others.

f. Install Display Expansion PCA in Backplane Assembly connector.

g. Install Top Plane Connector Assembly, part no. 02640-60022 on Display Expansion, DMA, Display Control, and Display Timing PCA connectors.

h. Check and, if necessary, adjust power supply in accordance with paragraph 3-10.

i. Depress TEST key and observe last line of test pattern for correct display enhancements. If enhancements are correct skip to step k. If adjustment is necessary, perform step j.

j. Perform brightness, half bright, focus, and field adjustments in accordance with paragraphs 3-11 and 3-12.

k. Firmly grasp mainframe top cover in one hand and release safety latch by pressing it inboard with other hand. Then, using both hands, carefully lower top cover to its closed position.

1-7. HP 13245A CHARACTER SET GENERATION KIT

The Character Set Generation Kit Accessory consists of a PROM Character PCA, part no. 02640-60053 and a Connector Assembly, part no. 02640-60070. Install the HP 13245A accessory as follows:

a. Open terminal to its half open position in accordance with paragraph 1-2.

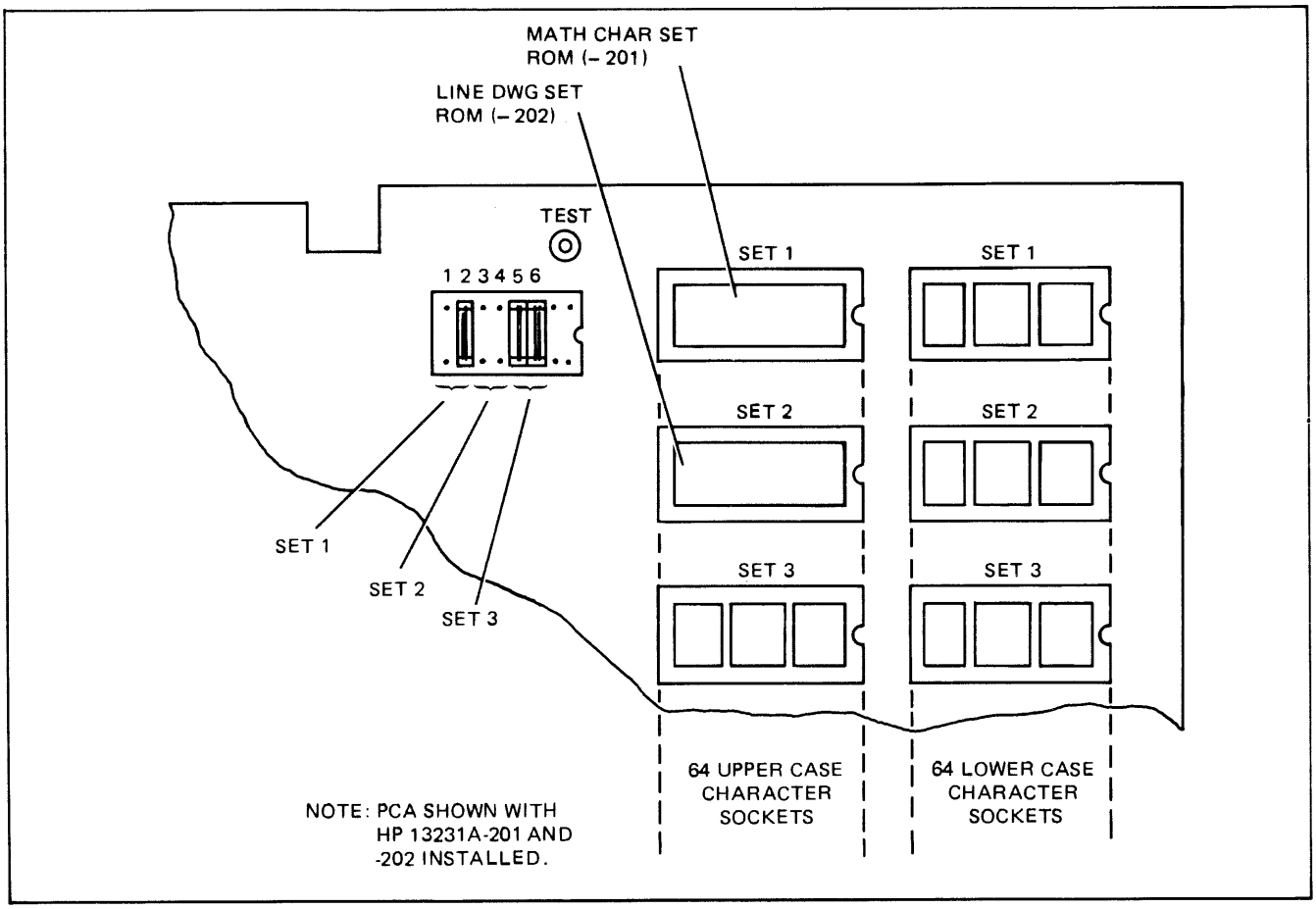

Figure 1-4. Display Expansion PCA Jumper and ROM Socket Locations

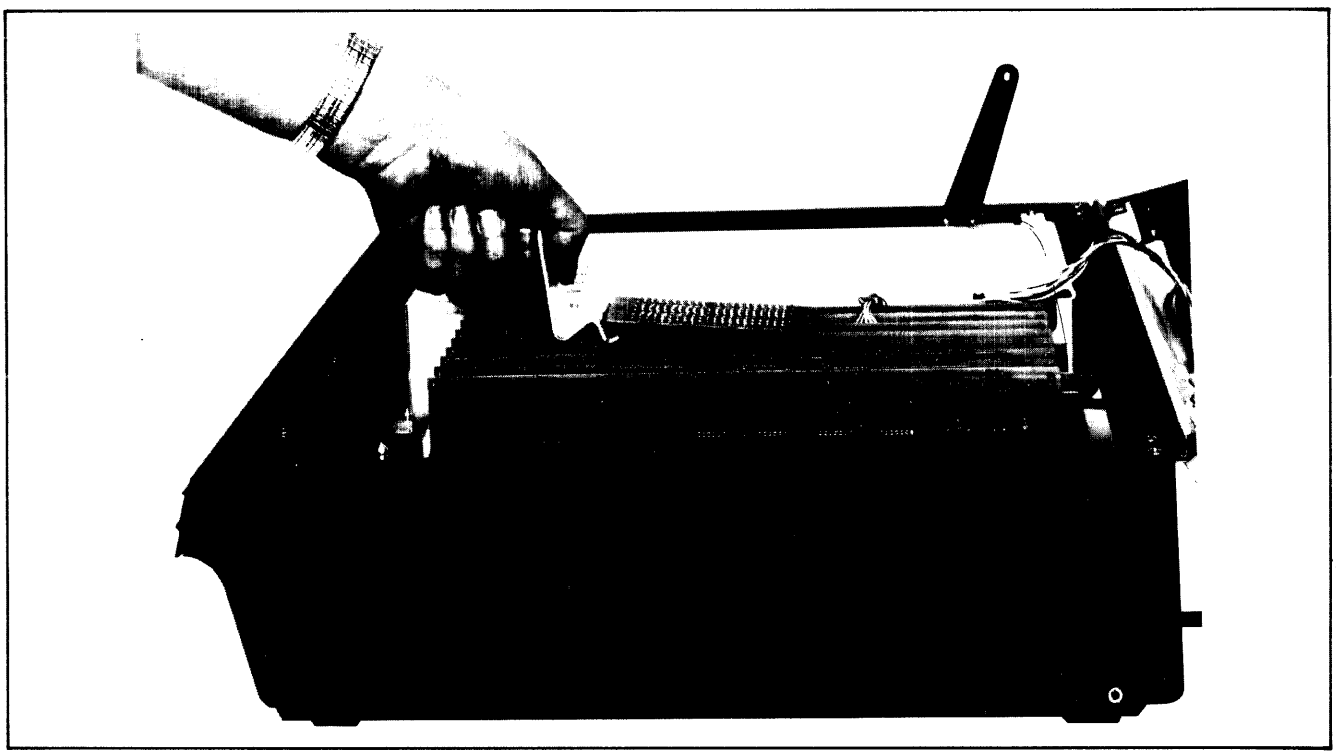

Figure 1-5. Top Plane Assembly Removal

b. Rearrange PCA's in the Backplane Assembly so that an unused connector is available for the PROM Character PCA adjacent to either the Display Control PCA or Display Expansion PCA depending on the character set(s) to be replaced. If the base character set is to be replaced, vacate a connector adjacent to the Display Control PCA. If an alternate character set(s) is to be replaced, vacate a connector adjacent to the Display Expansion PCA.

Note: PCA arrangement can be in any configuration with the following exceptions. The Keyboard Interface PCA should always be installed in one of the first five Backplane Assembly connectors closest to the power supply. The Display Expansion, DMA, Display Control, and Display Timing PCAs must always be installed as a group in adjacent connectors to accommodate the Top Plane Connector Assembly. The CTU Interface and Read/Write PCA's must always be installed in adjacent connectors. No Backplane Assembly connectors can be left vacant between any PCA's except for the two CTU PCA's which can be separated from the others.

c. Install PROM Character PCA in vacated Backplane Assembly connector.

Note: The base or alternate character set ROM(s) to be replaced by the user generated PROM set(s) must be removed from the applicable PCA in accordance with the instructions contained in the *Character Set Generation Kit Application Note*, part no. 13245-90001.

d. When connected to the Display Expansion PCA, the PROM Character PCA character sets 1 and 2 replace the Display Expansion PCA character sets 1 and 2, respectively. If an alternate set(s) is to be replaced, first determine if the user generated PROM set(s) is alphanumeric or microvector. Then, using table 1-1 and figure 1-4 as a guide, correctly arrange Display Expansion PCA jumpers 2 and 4 for the PROM character set type(s). (Jumpers 1 and 3 can either be removed or left installed.)

e. Attach Connector Assembly, part no. 02640-60070 between the two interface connectors (P2) on the PROM Character PCA and Display Control PCA or Display Expansion PCA.

f. Check and, if necessary, adjust power supply in in accordance with paragraph 3-10.

g. Firmly grasp mainframe top cover in one hand and release safety latch by pressing it inboard with other hand. Then, using both hands, carefully lower top cover to its closed position.

1-8. 64 CHARACTER LOWER CASE ROM

The 64 Character Lower Case ROM, part no. 1816-0613, is used to upgrade standard 64 character set terminals into Option 001 128 character set terminals. Install the ROM as follows:

a. Open terminal to its half open position in accordance with paragraph 1-2.

b. Insert connector removal tool under Top Plane Assembly as shown in figure 1-5 and remove Top Plane Assembly by pressing down on connector removal tool handle.

c. Locate and remove Display Control PCA from Backplane Assembly.

d. Using figure 1-6 as a guide, locate 128 CH W1 jumper sockets and solder in a jumper between W1 sockets.

e. Using figure 1-6 as a guide, locate upper case ROM U310 and vacant lower case ROM socket XU28.

f. Carefully insert 64 Character Lower Case ROM in socket XU28 so that ROM pin 1 is at upper right corner of XU28.

g. Reinstall Display Control PCA in Backplane Assembly connector from which it was removed.

h. Reinstall Top Plane Assembly on DMA, Display Timing, and Display Control PCA's top connectors.

i. Firmly grasp top cover in one hand and release safety latch by pressing it inboard with other hand. Then, using both hands, carefully lower top cover to its closed position.

1-9. HP 13236A CARTRIDGE TAPE

The HP 13236A accessory is provided to upgrade Option 008 terminals (standard terminals less mass storage capabilities) to standard terminals. This accessory consists of two Cartridge Tape Unit (CTU) Transport Assemblies, two Tape Cartridges, a CTU Interface PCA, a Read/Write PCA, a CTU Top Plane Assembly, a Motor Cable Assembly, a front bezel, and required attaching hardware. (Refer to table 4-1 for part numbers.) Figures 1-1 and 4-4 illustrate this accessory fully installed in the terminal and should be used as references for proper installation. Installation of this accessory requires the use of the HP CTU Tester, part no. 02640-60082 and the HP Checkout Cartridge, part no. 02640-60096. Install the accessory as follows:

a. Open terminal to its half open position in accordance with paragraph 1-2.

b. Remove four screws and lockwashers securing existing front bezel to mainframe shell. Remove and discard front bezel.

Note: To facilitate installation, removal, or service; it is recommended that accessory PCA's be installed in the second and third from last Backplane Assembly connectors

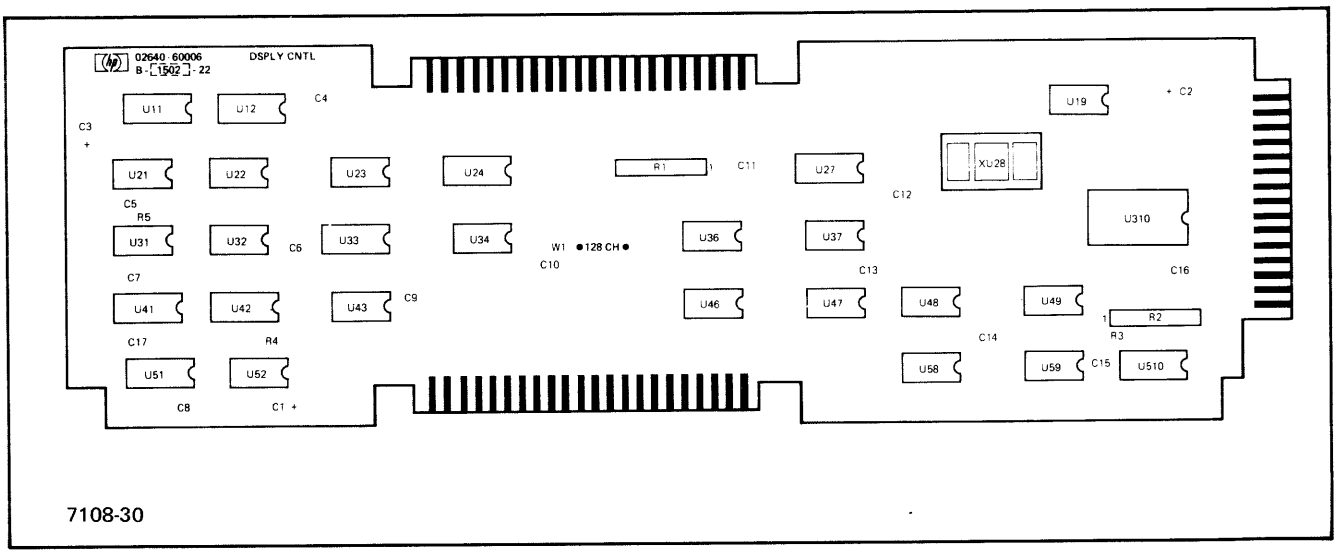

Figure 1-6. Display Control PCA Component Locations

whenever possible. This will provide maximum work space between the Read/Write PCA and right side of mainframe shell.

c. Ensure that CTU Interface PCA jumper configuration is as shown in figure 1-7 and, depending on available space, install PCA in next to last or third from last Backplane Assembly connector as shown in figure 1-1.

d. Connect Motor Cable Assembly's four-pin connector to Read/Write PCA's MOTOR connector J6. Connector J6 is located in upper right-hand corner of PCA.

e. Depending on position of CTU Interface PCA, install Read/Write PCA in last or next to last Backplane Assembly connector between CTU Interface PCA and right side of mainframe shell. The two PCA's must be installed in adjacent connectors with the Read/Write PCA closest to right side of mainframe.

f. Route Motor Cable Assembly to front of mainframe shell as shown in figure 1-1.

Note: The CTU Transport Assemblies are identical and interchangeable. Either assembly can be used for the following procedure.

g. Connect Motor Cable Assembly connector with red-white and black-white wires to CTU Transport Assembly motor connector.

CAUTION

It is imperative that all cable connections be made exactly as stated. Double check each connection. Incorrect connections will result in improper operation and may cause damage to the tape cartridges.

h. Check that two mounting screws, flat washers, and shock mounts are attached to CTU Transport Assembly as indicated in figure 4-4, index numbers 47, 48, 49, and 50.

Note: When installing the CTU Transport Assemblies, ensure that all cables are routed under and to the right of the assemblies along the bottom front of the mainframe shell.

i. Mount CTU Transport Assembly in the space provided for UNIT 0 (left-hand unit) by seating both shock mounts in the two mounting wells in the mainframe shell. Figure 1-1 shows the location of UNIT 0 and figure 4-4 illustrates the mounting well locations.

j. Tag CTU Cable Assembly 14-pin connector as Unit 0 for future reference.

k. Tighten two mounting screws into shock mounts seated in mounting wells until CTU Transport Assembly is firmly secured in place. Do not overtighten mounting screws. Overtightening mounting screws may cause misalignment between CTU Transport Assembly and front bezel.

l. Connect remaining Motor Cable Assembly connector (red and black wires) to remaining CTU Transport Assembly motor connector.

m. Repeat steps h through k except use UNIT 1 in lieu of UNIT 0.

n. Route both CTU Cable Assemblies along bottom right side of mainframe shell.

CAUTION

It is imperative that all cable connections be made exactly as stated. Double check each connection. Incorrect connections will result in improper terminal operation and may cause damage to tape cartridges.

Note: Each CTU Cable Assembly is color coded with a red stripe that extends visibly through the bottom of the assembly's 14-pin connector. When the cable assembly is properly connected to its associated connector socket on the Read/Write PCA, the red stripe is at the bottom of the PCA's connector socket.

o. Connect CTU Cable Assembly connector tagged "Unit ∅" to Read/Write PCA U∅ connector J5 and connect connector tagged "Unit 1" to U1 connector J4. Correct connections are shown in figure 1-1.

p. Check that four mounting screws and o-rings are attached to supplied front bezel as indicated in figure 4-4, index numbers 15, 16, and 17.

q. Carefully mount front bezel on mainframe shell so that both CTU Transport Assembly eject buttons protrude through the bezel holes.

r. Align four mounting screws with threaded holes in mainframe shell and secure bezel in place by tightening four screws.

s. Check for correct bezel and CTU Transport Assembly alignment by ensuring that both CTU eject buttons move freely within the bezel holes and that both bezel doors open and close without "hanging up" on the CTU Transport Assemblies.

t. If bezel and CTU Transport Assemblies are properly aligned, proceed to step u. If additional alignment is required, proceed as follows:

(1) Loosen misaligned CTU Transport Assembly mounting screws (two) until shock mounts are loosely seated in their respective mounting wells. When loose, the CTU Transport Assembly can be moved slightly in both its lateral and vertical planes.

(2) Manually move CTU Transport Assembly until properly aligned as stated in step s.

(3) While holding CTU Transport Assembly in properly aligned position, tighten two mounting screws until shock mounts firmly secure CTU Transport Assembly in place.

(4) Repeat substeps (1) through (3) as required until both CTU Transport Assemblies are properly aligned.

u. Clean and degauss both CTU Transport Assembly magnetic heads in accordance with paragraphs 3-16 and 3-17.

v. Install CTU Tester on top connectors of CTU Interface and Read/Write PCA's so that tester indicator lamps are closest to rear of terminal mainframe.

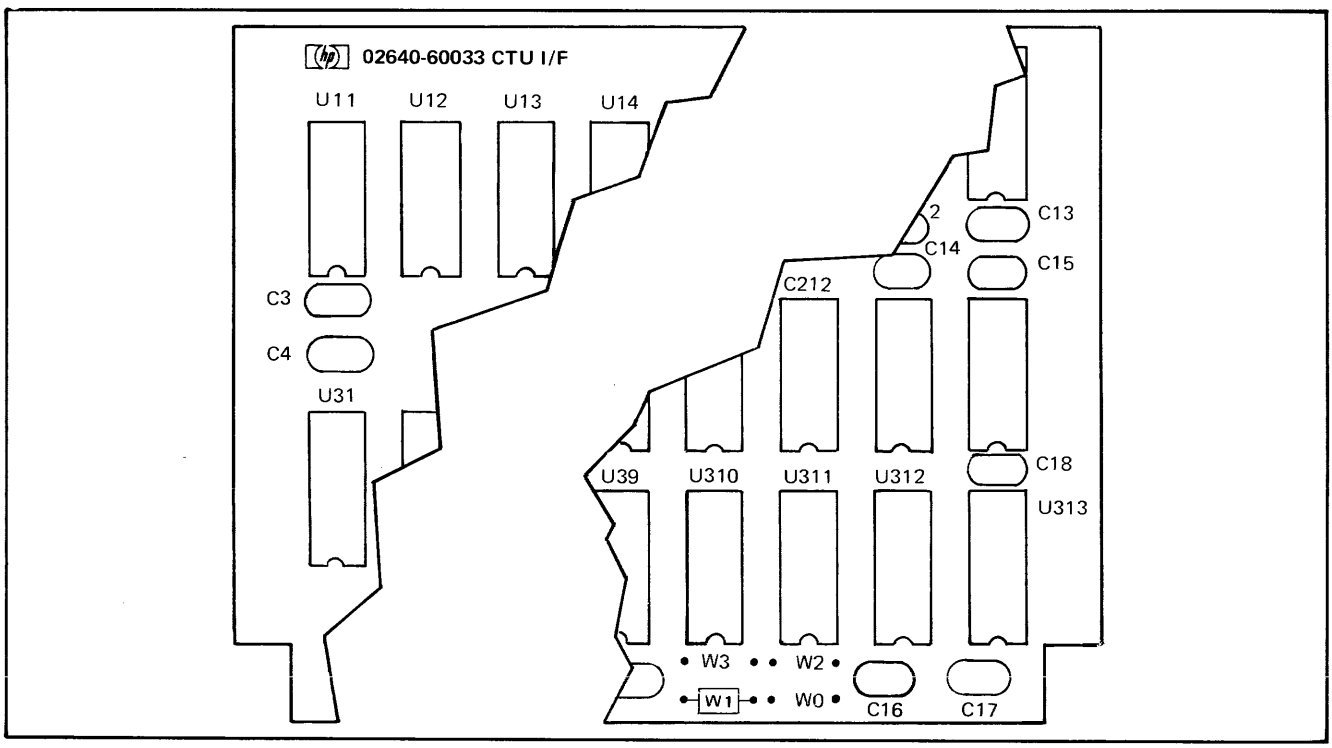

Figure 1-7. CTU Interface PCA Jumper Configuration

w. Set tester ON LINE/OFF LINE switch to ON LINE.

x. Check and, if necessary, adjust power supply in accordance with paragraph 3-10.

y. Check and adjust CTU Transport motor speed in accordance with paragraph 3-14, steps d through q.

z. Remove CTU Tester from CTU Interface and Read/Write PCA's and install CTU Top Plane Assembly on CTU Interface and Read/Write PCA's top connectors as shown in figure 1-1.

aa. Check accessory for proper operation in accordance with paragraph 3-7.

ab. Firmly grasp mainframe top cover in one hand and release safety latch by pressing it inboard with other hand. Then, using both hands, carefully lower top cover to its closed position.

1-10. SELECTING LINE VOLTAGE

The terminal can be operated from either 115 or 230V, 60 Hz line voltage (230V, 50 Hz optional). When shipped from the factory, the line voltage for which the terminal is configured is stamped on the mainframe rear panel identification label. If it is necessary to change the operating line voltage, ensure that power cord is disconnected and proceed as follows:

a. Open terminal to its half open position in accordance with paragraph 1-2.

b. Remove power supply housing (bottom left side of mainframe) by unlatching the two snap locks on front of housing and pulling housing up and out toward front of mainframe.

c. Using an access key or screwdriver, set voltage select switch S1 (see figure 1-1) to 115V or 230V as applicable.

d. Insert appropriate fuse for selected line voltage in rear panel fuse holder F1 and mark selected line voltage on identification label. (Use 4A, SB, 250V fuse for 115 or 230V, 60 Hz line voltage. Use 2A, SB, 250V fuse for 230V, 50 Hz line voltage.)

e. Check and, if necessary, adjust power supply in accordance with paragraph 3-10.

f. Replace power supply housing and secure in place with the two snap locks.

g. Firmly grasp mainframe top cover in one hand and release safety latch by pressing it inboard with other hand. Then, using both hands, carefully lower top cover to its closed position.

h. Perform terminal self-test.

1-11. SELECTING OPTIONAL OPERATING FUNCTIONS

The terminal is equipped with jumper selectable options that can be used to alter some of its operating functions. These options and their effects on terminal operation are discussed in paragraphs 1-12 through 1-19. To select an operating option, proceed as follows:

a. Open terminal to its half open position in accordance with paragraph 1-2.

b. Locate and remove Keyboard Interface PCA, part no. 02640-60019 from Backplane Assembly connector.

c. Using figure 1-8 as a guide, remove applicable jumper(s) from Keyboard Interface PCA jumper socket. Retain removed jumper(s) for possible future use.

d. Reinstall Keyboard Interface PCA in vacated Backplane Assembly connector.

e. Firmly grasp mainframe top cover in one hand and release safety latch by pressing it inboard with other hand. Then, using both hands, carefully lower top cover to its closed position.

f. Perform terminal self-test.

1-12. FUNCTION KEY TRANSMISSION OPTION

Normally, the Function Key Transmission Option is disabled (jumper A installed). Pressing such keys as ROLL UP, NEXT PAGE, etc., cause immediate execution of the function by the terminal but the applicable ASCII code for the function is not transmitted to the CPU. If Jumper A is removed, the ASCII codes for the functions are transmitted to the CPU as the keys are pressed and, if operating in half duplex, the function is also executed by the terminal.

1-13. SPACE OVERWRITE LATCH OPTION

Normally, the Space Overwrite Latch Option is disabled (jumper B installed) and the space overwrite latch is never set. In this case, when blanks (spaces) are entered into previously occupied character positions, the existing characters are overwritten. If jumper B is removed, the space overwrite latch is set by a carriage return and reset by a line feed, home, or horizontal tab. When set, blanks (spaces) typed or received are interpreted as cursor-right functions and and existing characters are not overwritten.

1-14. END-OF-LINE WRAP AROUND OPTION

Normally, the End-Of-Line Wrap Around Option is enabled (jumper C installed) and when a character is typed or received into column 80 of a line, the terminal automatically generates a carriage return and line feed, and the cursor is moved to the beginning of the next lower line. If jumper C is removed, an automatic carriage return and line feed is not generated at the end of each line and the cursor remains in column 80. Any subsequent characters typed or received replace the existing 80th character until some cursor movement function is typed or received that moves the cursor out of column 80.

1-15. BLOCK MODE OPTION

Normally, the Block Mode Option is disabled (jumper D installed) and the terminal is set for line-field operation.

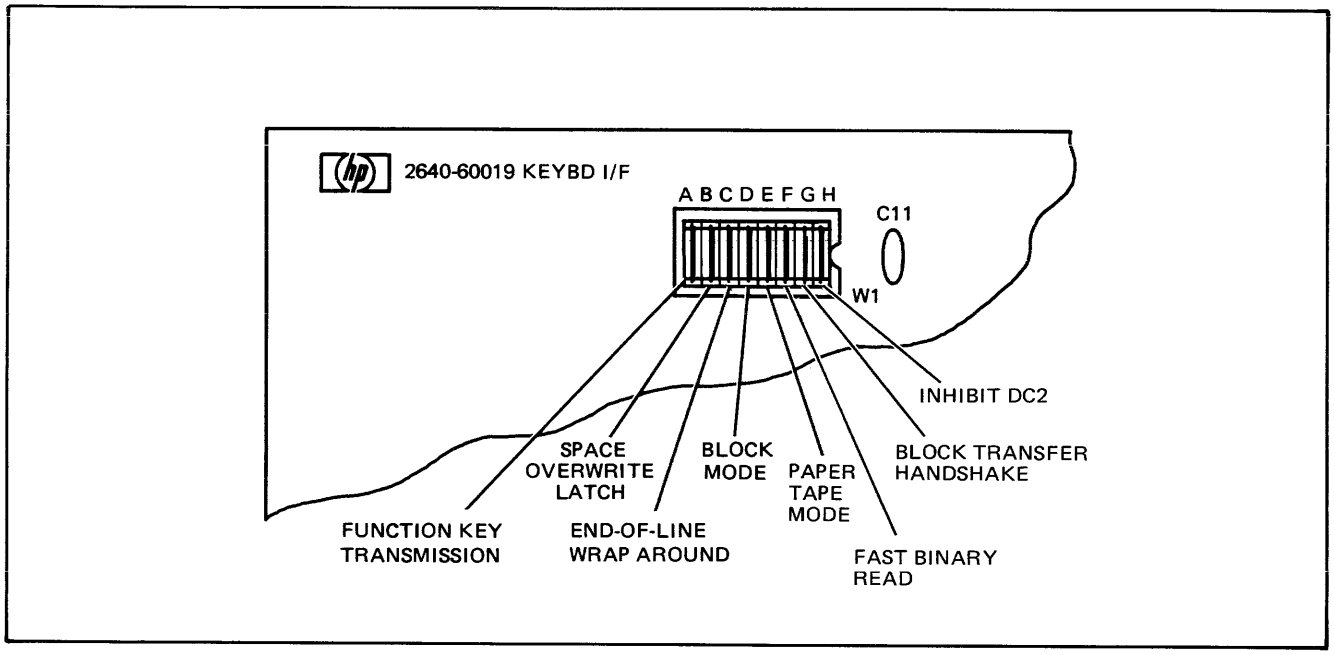

Figure 1-8. Keyboard Interface PCA Jumper Identifications

When set for line-field, all block transmissions are terminated by a carriage return followed by an optional line feed. If jumper D is removed, the terminal is set for page operation and all block transmissions are terminated with an RS. This jumper is ignored when the terminal is operated in Character Mode.

1-16. PAPER TAPE MODE OPTION

Normally, the Paper Tape Mode Option is enabled (jumper E installed) and, when the READ key is pressed and the AUTO LF key is latched down, each tape record is terminated by a carriage return. Then, after receipt of DC1, the next tape record is transmitted preceded by a line feed. If jumper E is removed, each tape record is terminated by a carriage return and line feed.

1-17. FAST BINARY READ OPTION

Normally, the Fast Binary Read Option is disabled (jumper F installed) and terminal transmission rate is controlled by the keyboard BAUD RATE switch. If jumper F is removed, terminal transmission rate is automatically switched to 9600 baud whenever an ESC e (Fast Binary Read) is received regardless of the BAUD RATE switch position.

1-18. BLOCK TRANSFER HANDSHAKE OPTION

Normally, the Block Transfer Handshake Option is disabled (jumper G installed) and, when operating in Block Mode, the terminal transfers data whenever a Q^C (Block Transfer Trigger DC1) is received. If jumper G is removed, all Block Mode transfers from the terminal are preceded by a R^C (Block Transfer Enable DC2). The terminal transmits DC2 upon receipt of DC1 and then waits for the receipt of a second DC1 before transmitting data. (Refer to paragraph 1-19.

1-19. INHIBIT DC2 OPTION

Normally, the Inhibit DC2 Option is disabled (jumper H installed) and, during Block Mode Hnadshake (paragraph 1-18), the terminal transmits a DC2 in response to a DC1 prior to transmitting data. If jumper H is removed, receipt of a DC1 is not required to trigger data transfers and DC2 is not transmitted during Block Mode Handshake transfers.

1-20. UNPACKING AND REPACKAGING FOR SHIPMENT

1-21. UNPACKING

The terminal has been carefully inspected and tested prior to shipment from the factory. Upon receipt, visually inspect the shipping carton for evidence of damage. If the shipping carton is damaged, request that the carrier's agent be present when the terminal is unpacked. Remove the terminal components from the shipping carton in accordance with the unpacking instructions listed below and check each item against the packing slip to ensure complete and correct delivery. Visually inspect all items for damage. If any of the items are damaged or fail to meet specifications, notify the carrier and the nearest Hewlett-Packard Sales and Service Office immediately. The HP Sales and Service Office will arrange for the repair or replacement of any damaged items without waiting for any claims against the carrier to be settled. Perform the unpacking instructions carefully so that the shipping carton can be retained for possible future use such as storage or reshipment of the terminal. The terminal may be shipped in either of two shipping cartons. To unpack your terminal, open top of shipping carton and, if cables, manuals, etc. are exposed, unpack in accordance with paragraph 1-22. If only an inner keyboard carton is exposed, unpack in accordance with paragraph 1-23.

1-22. UNPACKING METHOD 1. Unpack as follows:

a. Remove owner's manual, installation and service manual, power cord set, tape cartridges, head cleaning solvent, cleaning swabs, two mainframe access keys, data communication interface cable assembly and, if supplied, printer interface cable assembly.

b. Remove blue, plastic-covered preformed foam liner.

c. Remove keyboard and cable assembly.

d. Remove terminal mainframe.

e. Place preformed foam liner back inside shipping carton, close top cover, and retain shipping carton for possible future use.

f. Install the terminal in accordance with the instructions contained in the *HP 2644A Mini Data Station Owner's Manual*, part no 02644-90001.

1-23. UNPACKING METHOD 2. Unpack as follows:

a. Open top of exposed inner keyboard carton.

b. Remove first foam liner from keyboard carton.

c. Remove owner's manual, installation and service manual, head cleaning solvent, cleaning swabs, data communication interface cable assembly and, if supplied, printer interface cable assembly from keyboard carton.

d. Remove second foam liner from keyboard carton.

e. Remove Keyboard and Cable Assembly, Power Cord Set, tape cartridges, and two mainframe Access Keys from third foam liner in keyboard carton.

f. Replace two foam liners removed from keyboard carton and remove keyboard carton from shipping carton.

g. Remove cardboard tray from shipping carton.

h. Open top of floater carton and remove foam liner.

Note: The terminal mainframe is shipped in a plastic bag, face down (back of mainframe visible), inside the floater carton with a cardboard filler wedged between the bottom of the mainframe and the floater carton foam liner.

i. Determine bottom of mainframe by locating cardboard filler and carefully tip over entire shipping carton so that mainframe is setting upright.

j. Remove cardboard filler and carefully slide mainframe out of floater carton and shipping carton.

k. Remove mainframe from plastic bag.

l. Return entire shipping carton to its upright position.

m. Place plastic bag, cardboard filler, and foam liner back inside floater carton and close cover.

n. Place cardboard tray inside shipping carton on top of floater carton and set keyboard carton in tray.

o. Close top cover of shipping carton and retain for possible future use.

p. Install the terminal in accordance with the instructions contained in the *HP 2644A Mini Data Station Owner's Manual*, part no. 02644-90001.

1-24. REPACKAGING FOR SHIPMENT

1-25. SHIPMENT USING ORIGINAL PACKAGING. The same containers and materials used in factory packaging can be used for reshipment of the terminal. Alternatively, containers and packing materials can be obtained from Hewlett-Packard Sales and Service Offices. If the terminal is being shipped to the factory for servicing, attach a tag to the terminal specifying the return address, the type of service required, the terminal model number, and the full serial number of the terminal. Mark the carton "FRAGILE" to ensure careful handling. In any correspondence, refer to the terminal by model number and full serial number.

1-26. SHIPMENT USING NEW PACKAGING. The following instructions should be followed when packaging the terminal with commercially available materials:

a. Wrap the terminal in heavy paper or sheet plastic. If shipping the terminal back to the factory, first attach a tag to the terminal with the return address and indicate the type of service required, the terminal model number, and full serial number.

b. Use a strong shipping carton. A double-wall carton of 350-pound test material is adequate.

c. Ship the terminal mainframe face down in the shipping carton.

d. Use enough shock absorbing material (3- to 4-inch layer) on all sides of the terminal and keyboard to provide a firm cushion and to prevent movement inside the carton. Use particular care to protect corners, top of keyboard, and front of mainframe.

e. Seal the carton securely and mark it "FRAGILE" to ensure careful handling.

f. In any correspondence with the factory, refer to the terminal by model number and full serial number.

FUNCTIONAL OPERATION

SECTION II

2-1. INTRODUCTION

This section contains a block diagram level theory of operation discussion for the mini data station (terminal) and a pin-to-pin wiring diagram of the terminal.

2-2. GENERAL DISCUSSION

As shown in figure 2-1, the terminal basically consists of a power supply section, display section, memory section, control section, and input/output section. The interaction of these sections to provide the terminal's capabilities is discussed briefly in the following paragraphs. (A more detailed discussion is contained in paragraphs 2-3 through 2-34.

The power supply section consists of a Power Supply PCA and a Power Supply Control PCA that convert the primary power source into required operating voltages and basic clock pulses for the terminal. Except for the Sweep PCA, all interfacing between the power supply section and other terminal modules is provided by the Backplane Assembly.

The display section consists of a display controller subsection, Sweep PCA, CRT display, and, if installed, a Display Expansion PCA and PROM Character PCA. The display controller subsection generates all timing and control signals for the display section, provides drive signals for the Sweep PCA, initiates ASCII character (data) transfers from the memory section, and converts the ASCII characters into video drive signals. When installed, the Display Expansion PCA generates the required drive signals to add half bright, underline, and blinking display enhancements to the CRT and provides the capability for adding up to three additional 128 character sets to the terminal. (Refer to paragraph 1-7.) When installed, the PROM Character PCA provides the capability for adding up to two user generated character sets that can be used to replace the base character set on the Display Control PCA or two existing alternate character sets on the Display Expansion PCA. Set selection and data signal transfers between the PROM Character PCA and the Display Control or Display Expansion PCA's is provided by a separate connector assembly attached between the PCA's. The Sweep PCA is controlled by the Display Timing and Display Control PCA's (also the Display Expansion PCA when installed) and generates all drive signals, including filament and high voltages required by the CRT display. Timing and control signal interfacing between the display controller subsection modules (including the Display Expansion PCA when installed) is provided by the Top Plane Assembly. Data, associated transfer signals, and address interfacing between the subsection modules and other terminal modules is provided by the Backplane Assembly.

The control section is the central processing unit of the terminal and consists of the Processor and ROM PCA's. The Processor PCA fetches instructions from the operating system section of the ROM PCA and executes them; accessing the memory section, implementing input/output section modules or, if installed, implementing the Display Expansion PCA. In addition, the control section also controls and directs received byte information to the display section for translation from ASCII code into video signals. All signals interfacing between the control section and the other terminal modules is provided by the Backplane Assembly.

The memory section provides the operator with the usable RAM storage capability of the terminal. This section consists of the +4K Memory PCA. The +4K Memory PCA adds 4096 bytes of random access memory to the terminal. All read/write memory is accessed by the Processor PCA through the Backplane Assembly.

The input/output section is divided into a keyboard subsection, storage subsection, computer subsection, and peripheral subsection. All three subsections are implemented by the control section through the Backplane Assembly. The keyboard subsection consists of the Keyboard Assembly and Keyboard Interface PCA which provide direct data and instruction entry by the terminal operator. The storage subsection is a dual cartridge tape unit that provides data storage and retrieval capabilities for the terminal. The subsection consists of a Cartridge Tape Unit (CTU) Interface PCA, a Read/Write PCA, a CTU Top Plane Assembly, two CTU Transport Assemblies, and two or more tape cartridges. Each tape cartridge contains 140 feet of single-track 0.150 tape with a maximum formatted storage capacity of 128-K, eight-bit, data bytes. The dual cartridge tape unit provides full read and write capabilities in phase-encoded format. Data, associated transfer signals, and address interfacing between this subsection and other terminal modules is provided by the Backplane Assembly and CTU Interface PCA. The Read/Write PCA controls recording, reading, and tape motion of the two CTU Transport Assemblies. Interfacing between the two PCA's is provided by the CTU Top Plane Assembly and interfacing between the Read/Write PCA and the two CTU Transport Assemblies is provided by a Motor Cable Assembly and two CTU Cable Assemblies. The computer subsection consists of the Asynchronous Data Comm PCA and an interface cable assembly which provide a communication link between the terminal and an external computer. The peripheral subsection, if installed, consists of the Terminal Duplex Register PCA and an interface cable assembly which provide a communication link between the terminal and an external peripheral device such as a paper printer.

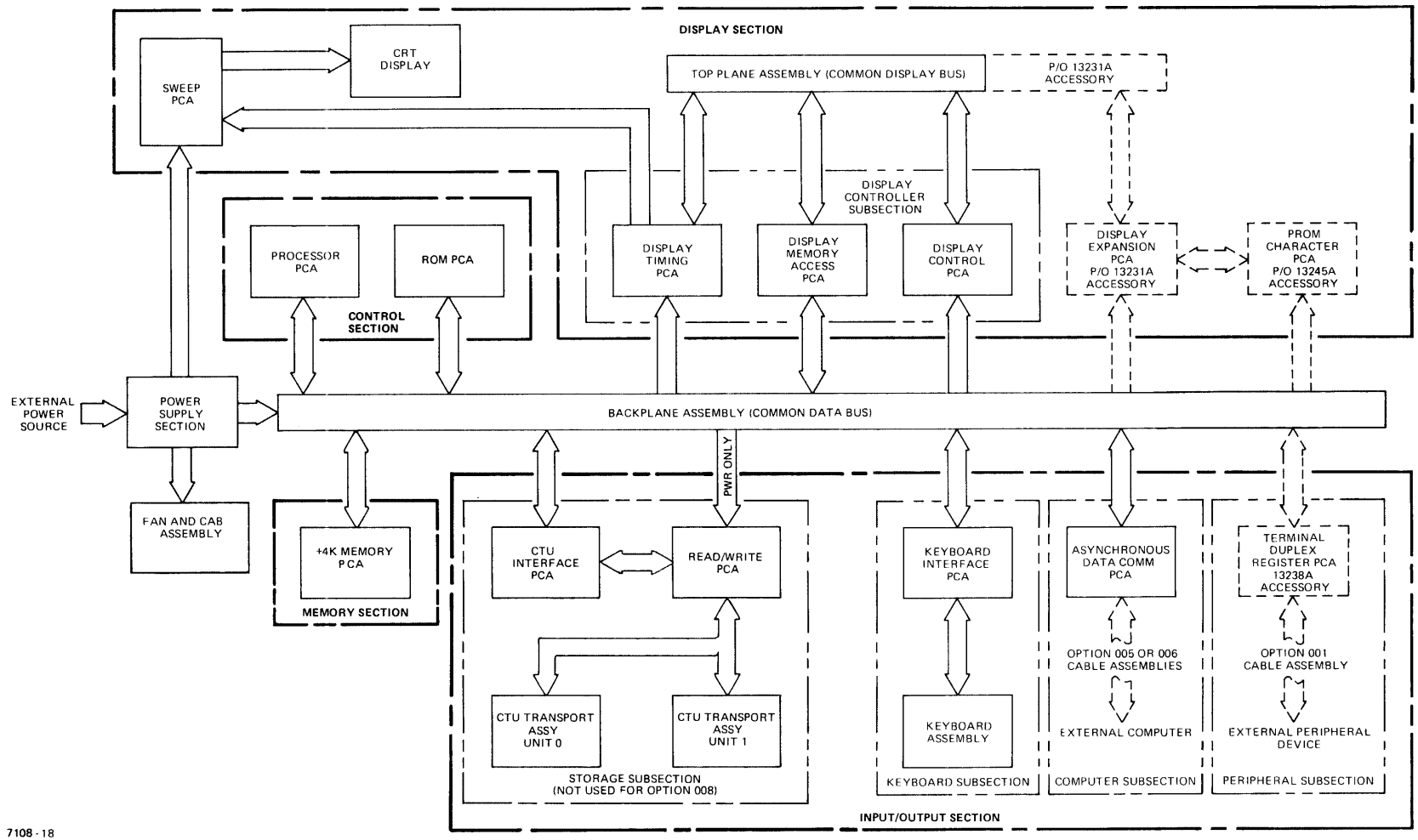

Figure 2-1. Basic Block Diagram

2-3. DETAILED DISCUSSION

The Functional operation discussion contained in the following paragraphs is keyed to the functional block diagram, figure 2-2. Figure 2-3 is a pin-to-pin wiring diagram of the terminal.

2-4. POWER SUPPLY SECTION

As shown in figure 2-2, the power supply section consists of a Power Supply PCA and a Power Supply Control PCA. The Power Supply PCA contains the voltage filter and conversion circuits and the Power Supply Control PCA contains the control, regulation, and basic system clock circuits.

The Power Supply PCA operates as a conventional chopped, choke-input supply and generates regulated +5V, +12V, -12V, and -42V supplies for distribution to the other terminal modules. The +5V, +12V, and -12V supplies are applied to the Backplane Assembly for common distribution while the -42V supply is applied exclusively to the Sweep PCA. All supplies are protected from overvoltage and reverse polarity by Zener diodes. The Power Supply PCA also provides voltage and current sensing for the Power Supply Control PCA monitoring circuits. The 115/230 voltage select switch is also located on this PCA.

The Power Supply Control PCA provides the basic system clock (4.915 MHz) for distribution to the other terminal modules through the Backplane Assembly, regulates and controls the power supplies, and provides a logic reset signal for common distribution through the Backplane Assembly each time the terminal is energized. Regulation of the power supplies is obtained by the generation of the alternating base drive signals applied to the Power Supply PCA which control the on and off times of the two chopper transistors. Control is obtained by monitoring the voltage and current sense lines from the Power Supply PCA and, if line voltage goes excessively low or primary current excessively high, disabling the base drive signals to shut down the supply. The +5V ADJ R14 potentiometer is also located on this PCA.

2-5. DISPLAY SECTION

The display section consists of a CRT display, Sweep PCA, display controller subsection and, if installed, a Display Expansion PCA and PROM Character PCA. Basically, this section converts ASCII characters into a visual display. The full display capability is 24 rows of 80 characters each. The standard terminal can display 64 different characters and has one display enhancement, inverse video. Accessories provide an additional 64 character ROM for 128 character operation, three additional display enhancements (half bright, underline, and blinking), and the capability for adding up to three 128- character sets. (A 64-character mathematic set ROM and 64-character line drawing set ROM are currently available from Hewlett-Packard.)

2-6. SWEEP PCA AND CRT. The Sweep PCA receives all required operating voltages and display signals via the Sweep Cable Assembly and applies generated drive signals and voltages to the CRT via the CRT Cable Assembly, Yoke Cable Assembly, and High Voltage Cable Assembly. As shown in figure 2-2, the Sweep PCA consists of video, vertical, and horizontal drive circuits, a voltage regulator circuit, and a high voltage power supply.

The vertical drive circuit receives and amplifies 60 Hz Vertical Drive signals (VDR) from the Display Control PCA and generates vertical deflection yoke drive signals for the CRT. This circuit also contains the HEIGHT R10 adjustment. The frequency of VDR is used to obtain the CRT 60 Hz frame rate. VDR goes low at the bottom of the CRT screen for one row time during which vertical retrace occurs. The screen is blanked during retrace by a Vertical Blanking signal (VBLNK) also generated by the Display Control PCA. The horizontal drive circuit receives 22.5 kHz Horizontal Drive signals (NHDR) from the Display Timing PCA and generates horizontal sweep drive signals for the CRT yoke. NHDR goes low at character column 81 to initiate horizontal retrace from right to left on the CRT screen. The screen is blanked during retrace by a Horizontal Blanking signal (HBLNK), also generated by the Display Timing PCA. Horizontal flyback pulses from this circuit are used as a source voltage for the high voltage power supply.

The video drive circuit receives Video signals (VIDEO) from the Display Timing PCA and Half Bright enhancement signals (NBHB) from the Display Expansion PCA accessory. These signals are combined and amplified to generate video drive signals for the CRT cathode. When VIDEO is high, the screen is on and, when VIDEO is low, the screen is off. When NBHB is high, full CRT brightness is displayed and, when NBHB is low, the half bright display enhancement is obtained. This circuit also contains the HALF BRIGHT R5 adjustment.

The voltage regulator circuit receives +5V, +12V, and -42V from the Power Supply PCA and provides voltage regulation and current limiting for the Sweep PCA. This circuit also contains the WIDTH R28 adjustment. The high voltage power supply rectifies and filters horizontal flyback pulses from the horizontal output transformer to generate +15 KV, +500V, +30V, and -100V for the CRT. The high voltage power supply circuit also contains the BRIGHTNESS R37 and FOCUS R33 adjustments.

2-7. DISPLAY CONTROLLER SUBSECTION. As shown in figure 2-2, the display controller subsection consists of a Display Control PCA, Display Timing PCA, and a Display Memory Access (DMA) PCA. The Display Control and Display Timing PCA's receive cursor position data from the Processor PCA and interact to generate drive signals for the Sweep PCA, initiate data transfers from the memory section to the DMA PCA, and to convert received ASCII characters into video signals for the Sweep PCA. The DMA PCA, under control of the Display Control and Display Timing PCA's, addresses the memory section, reads data from the memory section, and alternately refreshes and transmits received data for the Display Control and Display Expansion PCA's.

2-8. Basic Timing. Except for the DMA PCA bus cycle logic which use the 4.915 MHz System Clock (SYS CLK), all timing for the display section is derived from the Display Timing PCA 21.06 MHz display controller clock (CLK) which is the frequency at which character dots are written onto the CRT screen. As shown in figure 2-2, CLK is applied directly to the Display Expansion PCA (paragraph 2-15) and Display Control PCA dot generator. The dot generator is a nine-bit ring counter that divides CLK by nine and generates timing signals D0 through D8 that correspond to particular dot times within the character cell. D0 is used to clock the cursor generator and a 104-column counter which defines 104 character columns. The CRT displays 80 of these columns. The remaining 24 column counts occur during horizontal retrace. The seven-bit output (horizontal column bits) of this counter is applied to the video logic along with timing signals D0, D2, D6 and D8 and column count 103 (N103) to derive Horizontal Drive (NHDR) for the Sweep PCA, Horizontal Blank (HBLNK) for the video generator logic, Circulation (0CIRC) and Circulation Enable (0CIRCEN) for the DMA and Display Expansion PCA's, Buffer Clock (BUFCLK), and Vertical Clock (VRTCLK). BUFCLK is the 2.34 MHz display enhancements clock. VRTCLK is used to clock scan line counters on the Display Expansion and Display Control PCA's. These counters define the 15 individual scan lines of a row for the character ROM's. The line count outputs (LC0 through LC3) are applied to the character generator (four least significant address bits) and to the cursor line enable logic to derive Cursor Line Enable (CLEN) and Line Count 11 (L11) for the video generator logic and Line Count 14 (N14). N14 is applied to a divide-by-25 row counter to define 25 separate rows. The CRT displays 24 of these rows. The remaining row count occurs during vertical retrace. The five-bit output of the row counter is applied to the video logic along with N103 to derive Vertical Drive (VDR) for the Sweep PCA, Vertical Blank (VBLNK) for the video generator logic, interrupt Set (INT SET) SET) for the DMA and Display Expansion PCA's, and 60 Hz Gated Vertical Sync (GVS). GVS is applied to the DMA PCA (paragraph 2-14) and to a counter in the Display Timing PCA which divides the frequency by 12 to obtain a 5 Hz clock for the blink generator. The blink generator provides the 2.5 Hz Cursor Blink (CBL) and 1.25 Hz Enhancement Blink (BLINK) signals for the video generator logic.

2-9. Character Generation. The seven-bit ASCII code (NBIT0 through NBIT6) from the DMA PCA (paragraph 2-12) is applied to the Display Control PCA character generator which consists of either an upper-case 64-character set ROM or an upper-case 64-character set ROM and a lower-case 64-character set ROM. The ROM's generate dot patterns corrsponding to received ASCII codes. (Refer to paragraph 2-15 and 2-18.) NBIT5 and NBIT6 are first applied to the character select logic which determines if the generated character will be upper or lower case by enabling the applicable ROM. It should be noted that the 128 CH jumper located in this circuit must be installed if upper and lower case (128 characters) operation is desired and must be removed for upper case only (64 characters) operation. The character generator, under control of the character select logic, receives its six most significant bits of address (MSB) from the DMA PCA (NBIT0 through NBIT4 and NBIT6) and four least significant bits of address (LSB) from the divide-by-15 line scan counter (LC0 through LC3). Each output from the character generator is an eight-bit dot position word (DBIT0 through DBIT7). DBIT1 through DBIT7 correspond to the seven character dot positions and are applied to the parallel-to-serial converter for conversion into a serial bit stream (NBITS) for the video generator logic. The eighth bit (DBIT0) is applied to the dot shift generator as a normal/delay shift control signal. The dot shift generator provides a half shift capability of the character dot positions which enhances character resolution by producing smoother angles and curves. Depending on the logic level of DBIT0, the dot shift generator Shift Clock (SHFT CLK) output shifts DBIT1 through DBIT7 out of the converter either unshifted (DBIT0 = 1) or delayed one-half dot time (DBIT0 = 0) which shifts the character dots on the CRT screen to the right one-half dot width.

2-10. Cursor Generation. The position of the cursor on the CRT screen is controlled by the Processor PCA. When a new position is required, the position ($\overline{BUS0}$ through $\overline{BUS6}$) along with a blanking bit ($\overline{BUS7}$) is applied to the "X" and "Y" holding registers. The holding register contents are constantly being compared in their respective comparators against the position of the character being written on the screen. Instruction and address signals are applied to the bus decoder network to derive the Cursor "X" Strobe (NCXS) and Cursor "Y" Strobe (NCYS) signals for the holding registers and blink generator. NCXS and NCYS are used to clock the new "X" and "Y" cursor positions from the holding registers to the "X" and "Y" comparators. NCYS also clocks Screen Blanking (NBLNK) from the "Y" holding register into the video generator logic. NCXS also momentarily inhibits CBL from the blink generator whenever the cursor is repositioned. The "X" comparator compares the seven "X" position bits against the character column position bits from the 104-column counter and applies a Cursor "X" Enable (CXEN) signal to the cursor generator whenever a compare exists. The "Y" comparator compares the five "Y" position bits against the character row position bits from the row counter and applies a Cursor "Y" Enable (CYEN) signal to the cursor generator whenever a compare exists. The cursor line enable logic monitors the scan line counter and decodes line count 11 and 12 to generate Cursor Line Enable (CLEN) for the cursor generator. Upon receipt of CXEN, CYEN, and CLEN, the cursor generator applies a Valid Cursor (VCSR) signal to the video generator logic.

2-11. Composite Video Generation. The Video (VIDEO) serial bit stream is generated by the composite generator logic tree and is applied directly to the Sweep PCA. Except for the Half Bright (NBHB) signal which is applied directly from the Display Expansion PCA to the Sweep PCA, all display enhancements, base and alternate character serial bit streams, horizontal and vertical blanking signals, and cursor position signals are combined by this generator. The Inverse Video (IV) signal is generated by the Display Timing PCA and is initiated by the Inverse

Video Select (NIV) signal from the DMA PCA. The Blinking Video (NBBL), Underline Video (NBUL), and Alternate Character (NXBITS1) signals are supplied by the Display Expansion PCA. All other video generator inputs have been discussed previously.

2-12. Character Refreshing. The DMA PCA refresh operations are initially controlled by INT SET from the Display Control PCA and bit 6 ($\overline{BUS6}$) of the cursor ("Y" position from the Processor PCA. When $\overline{BUS6}$ is 0, the DMA flip-flop is set (DMA ON) which enables the bus cycle logic discussed in paragraph 2-14. INT SET resets the 80-character counter whose output (80) is then combined with DMA ON to initiate the transfer of 80 characters from the memory section. The bus cycle logic clocks received data ($\overline{BUS0}$ through $\overline{BUS7}$) through the holding registers into one of two 80-character shift registers and their respective line buffers. Register and line buffer selection is determined by the EVEN signal from the Display Control PCA applied to the refresh logic which generates the EVEN and $\overline{EVEN}$ enabling signals and their corresponding clocks. While LOAD from the display function logic is loading a row of data into one line buffer, 0CIRC and 0CIRCEN from the Display Timing PCA are rotating the contents of the other shift register at 2.34 MHz to supply one character out of its buffer every nine dot positions as determined by clock D1 from the Display Control PCA. At the end of each row (80 characters), the load/refresh functions of the registers and corresponding buffers are reversed. Buffer outputs NBIT0 through NBIT6 are applied to the Display Control PCA as previously discussed and, if installed, to the Display Expansion PCA. The eighth bit, NIV, is applied to the Display Timing PCA as previously discussed.

2-13. Display Function Control. As received data from the memory section is clocked through the holding registers, it is edited by the display function priority encoder which applies a three-bit function code to the display function decoder. Depending on its input, the display function decoder applies a Control, Character, End-of-Line (EOL), End-of-Page (EOP), or Link function control signal to the display function logic. The display function logic, under control of the bus cycle logic, initiates execution of the decoded function. When a control function is decoded, the display function logic generates a Line Buffer Load (LBLOAD) signal which clocks the inverse video bit ($\overline{BUS1}$) into the line buffers and/or clocks other enhancement or alternate character select bits ($\overline{BUS0}$ and $\overline{BUS2}$ through $\overline{BUS5}$) through the Display Expansion PCA holding registers. (Refer to paragraph 2-15.) When a character function is decoded, a LOAD clock signal is generated for the refresh logic as previously discussed. When an end-of-line or end-of-page function is decoded, an EOL or EOP signal is applied to the upper and lower byte address registers to cause the remainder of the current line or page to be written with blanks. When a link function is decoded, the display function logic applies a LINK signal to the address registers which fetches the next byte of data from the memory section. The LINK plus the last byte become the next location address from which data is to be read.

2-14. Bus Cycle Control. The bus cycle is a six-state sequence controlled by the bus cycle logic. At the beginning of each new page of displayed data (bus cycle idle state), GVS resets the byte address registers to the starting address of the memory section and INT SET resets the 80-character counter. This initiates the second state of requesting control of the data bus. During this state, if Priority In (PRIOR IN) is high and no functions are being executed, the bus cycle logic advances to state three of getting the bus and to state four of requesting data. During this state, the contents of the byte address registers and a Request ($\overline{REQ}$) signal are applied to the memory section. If the display function logic is executing an end-of-line or end-of-page operation at this time, $\overline{REQ}$ is inhibited until the end of 80 characters or 24 rows, respectively. Once the memory section decodes its address from the byte address registers, the bus cycle logic advances to state five and data is clocked through the holding registers for decoding as discussed in paragraph 2-13. During this state, the bus cycle logic also decrements the byte address registers. During decoding, the bus cycle logic advances to state six, releases control of the bus, and returns to its idle state until INT SET is again applied to signal the start of another new line. After 24 lines have been fetched from the memory section, GVS is again applied and the complete cycle is repeated.

2-15. DISPLAY EXPANSION PCA. The Display Expansion PCA provides three additional display enhancements and the capability for adding up to three 128-character sets for the display section. All timing and control signals for this PCA are received from the dispaly controller subsection as previously discussed.

2-16. Character Generation. As shown in figure 2-2, the same seven-bit ASCII code (NBIT0 through NBIT6) applied to the Display Control PCA from the DMA PCA (paragraph 2-12) is applied to the three 64/128 character set ROM's (if installed) on the Display Expansion PCA. These ROM's, if selected, generate dot patterns corresponding to received ASCII codes the same as the base character set ROM(s) on the Display Control PCA. NBIT5 and NBIT6 are first applied to the character select logic which determines whether the character will be generated by the upper or lower case ROM's of the selected character set. (Refer to paragraph 2-17.) It should be noted that jumpers are also contained in this circuit that must be properly configured for 64- or 128-character operation and for operating with alphanumeric and microvector sets. (Refer to paragraph 1-6.)

Once selected, the character set ROM's receive their six MSB (NBIT0 through NBIT4 and NBIT6) from the DMA PCA and four LSB (LC0 through LC3) from the divide-by-15 line scan counter. This counter is clocked by VRTCLK and reset by N14 the same as the Display Control PCA counter discussed in paragraph 2-8. The output of the character set ROM's is either an eight-bit or nine-bit dot position word (DBIT0 through DBIT7 or DBIT0 through DBIT8) that is applied to the shifter logic and parallel-to-serial converter for conversion into a serial bit stream (NXBITS1). If the selected character set is an alphanumeric ROM(s), its output is an eight-bit word that is shifted out

of the parallel-to-serial converter under control of the shifter logic as discussed in paragraph 2-9. (Seven-bit data word with each bit shifted or unshifted as determined by DBIT0.) If the selected character set is a microvector ROM(s), its output is a nine-bit word, the half shift capability of the shifter logic is disabled, and DBIT0 and DBIT8 are merged into NXBITS1 along with DBIT1 through DBIT7. The character set encoder receives Sense signals (1SN, 2SN, and 3SN) from the character sets to interpret whether or not the selected set is an alphanumeric or microvector set. This signal is determined by the jumper configurations discussed in paragraph 1-7. The signal must be low (jumper installed) for alphanumeric operation and high (jumper removed) for microvector operation. During alphanumeric operation, the character set encoder enables the shifter logic half shift capability as previously discussed. During microvector operation, the half shift capability is disabled and the shifter logic merges DBIT0 and DBIT8 into the serial bit stream along with the output from the parallel-to-serial converter.

2-17. Character Set and Display Enhancement Selection. The character set selection bits ($\overline{BUS4}$ and $\overline{BUS5}$) and display enhancement selection bits ($\overline{BUS0}$, $\overline{BUS2}$, and $\overline{BUS3}$) are clocked through the holding register by LBLOAD from the DMA PCA (paragraph 2-13) into the line buffers. The refresh and load logic, when enabled by LOAD from the DMA PCA, alternately loads and refreshes the line buffers by using the EVEN, 0CIRC, 0CIRCEN, LOAD, D1, and Buffer Select (BSEL) signals as discussed in paragraph 2-12. The line buffers set select outputs (NBSS0 and NBSS1) are decoded by the character set decoder and generates Set Enabling signals (1SEN, 2SEN, and 3SEN) for the appropriate character set ROM(s). (Refer to paragraph 2-18.) NBSS0 and NBSS1 are also applied to the Display Control PCA to enable or disable the base character set. If either signal is high, the base set is disabled by NE1, and the character set decoder enables the selected alternate character set. Display enhancement selection is determined by the logic levels of $\overline{BUS0}$, $\overline{BUS2}$, and $\overline{BUS3}$. When high, these bits become Underline Enable (ULEN), Half Bright Enable (HBEN), and Blinking Enable (BLEN) signals and are applied to the enhancement generator along with BUFCLK and 0CIRC clocks. Once enabled, the enhancement generator applies the selected enhancement signal(s) (NBHB, NBBL, and/or NBUL) to the Sweep PCA and Display Timing PCA as previously discussed. This circuit also contains the FIELD adjustment.

2-18. PROM CHARACTER PCA. The PROM Character PCA provides the capability for adding up to two user generated PROM character sets as described in the *HP Character Set Generation Kit Application Note*, part no. 13245-90001. When installed, the PROM Character PCA is connected directly to either the Display Control or Display Expansion PCA depending on the character set(s) to be replaced. The number of PROM character sets installed on the PCA depends upon the user application and design as does the number of PROM's contained in each set. Each 64 character set requires two PROM's; a 128 character set requires four PROMs; and, if the set is a microvector type, five PROM's are required. When the PROM Character PCA is connected to either the Display Control or Display Expansion PCA, the PROM character set(s) replaces the ROM character set(s) normally mounted on that PCA. It should be noted that the ROM character set(s) to be replaced must be removed from its PCA to obtain proper operation.

2-19. Character Set Selection. As shown in figure 2-2, character set selection is determined by the PROM Character PCA character set decoder. When the PCA is connected to the Display Control PCA, the Base Character Set Select signal (NSET0) is always low and the character set decoder applies four Base Set Enable signals (0/1SEN) to the PROM's in character set 0. Alternate character set select signals (NBSS0 and NBSS1) are also applied to the character set decoder and, if either or both signals go low, the character set decoder disables the PROM set by removing 0/1SEN. When this occurs, character set selection and character generation is performed by the Display Expansion PCA as discussed in paragraphs 2-16 and 2-17. When the PROM Character PCA is connected to the Display Expansion PCA, NSET0 is always high and NBSS0 and NBSS1 are decoded by the character set decoder into Set Enabling signals (0SEN and 1SEN or 2SEN) for the PROM's in character set 1 or 2. It should be noted that the character set decoder generates three enabling signals for the PROM sets when replacing Display Expansion PCA alternate character sets. This provides for the enabling of the fifth PROM required by the microvector type character sets.

2-20. Character Set Generation. Once enabled, the PROM character set(s) function the same as the replaced ROM character set(s) to generate dot patterns corresponding to received ASCII codes. (Refer to paragraphs 2-9 and 2-16.) BIT5 and BIT6 are applied to the character select decoder which determines individual PROM selection(s) within each character set. (BIT5 and BIT6 perform the same function for the character set encoder when a microvector character set is installed.) It should be noted that when a PROM set is used to replace an alternate character set that the Display Expansion PCA jumpers must be arranged to meet the requirements of the PROM character set configuration. Once selected, the character set PROM's receive their five MSB from BIT0 through BIT4 and their four LSB from LC0 through LC3. The PROM set output (DBIT0 through DBIT7) is an eight-bit dot position word that is applied back to the parallel-to-serial converter of either the Display Control or Display Expansion PCA. (DBIT0 provides shift control as previously discussed in paragraphs 2-9 and 2-16.) If a microvector character set is installed, the required fifth PROM of the set applies four Sensing output signals (1SN or 2SN) to the character set encoder which, along with BIT5 and BIT6, cause the generation of DBIT8 required for microvector character generation.

2-21. CONTROL SECTION

The control section consists of the Processor PCA and ROM PCA. As shown in figure 2-2, the Processor PCA contains the central processing and control logic and the ROM PCA contains the 12K of ROM necessary for storing the basic operating system firmware.

2-22. MICROPROCESSOR. The microprocessor accesses and executes instructions stored in ROM. The microprocessor instruction set consists of 48 instructions including data manipulation, binary arithmetic, and jump to subroutines. The microprocessor communicates over an eight-bit data and address bus under control of the bus cycle logic. Three STATUS outputs to the cycle decoder are used to indicate the state of the microprocessor at any time during the execution of an instruction cycle. The cycle decoder constantly monitors the STATUS lines and generates the ENABLE signals for the bus cycle logic, the T1I acknowledge signals for the interrupt generator, and the Upper and Lower Byte Clocks (UBCL and LBCL) for the address registers at the times required to coincide with the microprocessor operations. An Interrupt (INT) control signal from the interrupt generator is used to reset the microprocessor to the beginning of the ROM program. Two non-over-lapping clocks (PCL) from the clock generator are required to drive the microprocessor.

A typical instruction cycle consists of five states; T1 through T5. During T1 and T2 states, an address is sent to its address bus for addressing memory or an I/O module such as the DMA or Asynchronous Data Comm PCA. During T3 state, an instruciton or data from memory or an I/O module can be received through the data bus. If an instruction is received, it is executed during T4 and T5 states. If an internal execution is not required, states T4 and T5 are omitted. If the terminals data bus is busy ($\overline{BUSY}$ low), the microprocessor goes into a Wait state until the bus is free. If an INT is received, the cycle is interrupted and acknowledged by replacing state T1 with state T1I. Instructions can require from one to three cycles for complete execution. The first cycle is always an instruction fetch cycle. The second and third cycles are for reading data, writing data, or I/O operations. The cycle types are indicated by BIT6 and BIT7 present on the data and address bus during state T2.

2-23. BUS CYCLE CONTROL. Before the microprocessor can access memory, it must have control of the terminals data bus. This is accomplished by the bus cycle logic which is synchronized with the instruction set by clocks ϕ11, ϕ12, and SYNC. Each bus cycle is a six-state sequence. At the beginning of each new instruction cycle (microprocessor state T1 and bus cycle Idle state), the cycle decoder applies an ENABLE signal to the bus cycle logic. This initiates the second bus cycle state of requesting control of the data bus. During this state, if PRIOR IN is high and the data bus is free ($\overline{BUSY}$ high), the bus cycle advances to state three of getting the bus and to state four of sending Request ($\overline{REQ}$) to the memory section or an I/O module. During these states, the contents of the address registers are strobed onto the data bus along with $\overline{REQ}$. It should be noted that two bus transfer signals ($\overline{I/O}$ and $\overline{WRITE}$ are applied to the bus along with the address signals. The combined logic levels of these two signals specify whether a read memory, write memory, input, or output bus transfer is to take place. During read cycles, $\overline{REQ}$ is applied to the data bus during microprocessor T2 state and requested data is received during T3 state. During write cycles, $\overline{REQ}$ is applied to the bus during microprocessor T3 state. Once the bus transfer is executed, the bus cycle advances through state five to state six, releases control of the data bus, and returns to its Idle state until ENABLE is again applied from the cycle decoder.

2-24. INITIAL START UP. When power is first applied to the terminal, it is detected by the interrupt generator which applies INT to the microprocessor. Upon receipt of INT, the microprocessor goes from its Halt or Wait state to its T1I state. This is monitored by the cycle decoder which applies T1I Acknowledge back to the interrupt generator. Upon receipt of T1I, the interrupt generator applies RESTART to the restart logic which applies the restart instruction to the microprocessor. This causes the microprocessor to fetch its next instruction from ROM memory location zero and the program begins. From here, the program can go anywhere in the available memory space. It should be noted that in order for the restart instruction to cause the microprocessor to jump to memory location zero, that the Attention ($\overline{ATT}$) signal from the Asynchronous Data Comm PCA must be low. If $\overline{ATT}$ is high, the restart logic changes the restart instruction into a microprocessor subroutine load instruction.

2-25. ROM PCA. As shown in figure 2-2, the ROM PCA contains 12K of ROM, an address comparator, a ROM select decoder, and associated timing and control logic. The 12K of ROM is a 12K by 8 array that is enabled in 2K by 8 modules. The basic operating system is stored in ROM. The address comparator applies a high Valid Address signal (ADDR) to the ROM select decoder whenever a ROM address within the assigned memory space is recognized. ADDR is determined by the combination of the address jumper configurations and the two most significant address bits ($\overline{ADDR14}$ and $\overline{ADDR15}$). The ROM select decoder, when enabled, decodes the logic levels of $\overline{ADDR11}$ through $\overline{ADDR13}$ and applies a corresponding Select signal (SEL) to the appropriate 2K module of ROM. The remaining address bits ($\overline{ADDR0}$ through $\overline{ADDR10}$) are applied directly to the memory modules. It should be noted that each 2K module of ROM has an associated jumper that must be installed in order for the SEL signal from the decoder to be recognized. The ROM select decoder is enabled whenever ADDR is high and the two ENABLE signals from the timing and control logic are low.

The timing and control logic, in conjunction with three address control signals ($\overline{REQ}$, $\overline{WRITE}$, and $\overline{I/O}$) from the Processor PCA, initiates and controls the memory access cycle. To initiate an access cycle, $\overline{I/O}$ and $\overline{WRITE}$ must be high and $\overline{REQ}$ must be low. When high, $\overline{I/O}$ and $\overline{WRITE}$ generate the two required ENABLE signals for the ROM select decoder. When $\overline{I/O}$ is low, memory access is inhibited while the Processor PCA is writing or reading to an I/O module such as the Keyboard Interface or Cartridge Tape Unit Interface PCA's. The timing and control logic combines any decoded ROM SEL signal with $\overline{REQ}$ (low) and SYS CLK and generates Read Address (READ ADDR), Output Enable (OUT EN), and $\overline{WAIT}$. READ ADDR is required to allow data to be read from the addressed ROM and OUT EN gates the eight-bit byte (ROM DATA) from ROM through the bus drivers onto the data bus. The generated $\overline{WAIT}$ signal is low while a memory cycle is in progress and goes high when each cycle is completed.

2-26. MEMORY SECTION

The memory section consists of the +4K Memory PCA that provides 4,096 words of addressable read/write storage. As shown in figure 2-2, the +4K Memory PCA contains an address comparator, 4K of RAM, an address multiplexer and buffers, refresh logic, and associated timing and control logic. The address comparator applies ACS REQ to the timing and control logic whenever a RAM address within the assigned memory space (selected by the address configuration network) is recognized. ACS REQ is determined by the combination of the address jumper configurations and the four most significant address bits ($\overline{\text{ADDR12}}$ through $\overline{\text{ADDR15}}$. The remaining address bits ($\overline{\text{ADDR0}}$ through $\overline{\text{ADDR11}}$) are applied to the memory chips through the address multiplexer and address buffers. Three address control signals ($\overline{\text{REQ}}$, $\overline{\text{WRITE}}$, and $\overline{\text{I/O}}$) are also applied to the timing and control logic. As previously discussed in paragraph 2-25, $\overline{\text{REQ}}$ must be low and $\overline{\text{I/O}}$ must be high to start a memory access cycle and the logic level of $\overline{\text{WRITE}}$ determines if a read or write cycle is to be initiated. When $\overline{\text{WRITE}}$ is high, a read from memory cycle is initiated and, when $\overline{\text{WRITE}}$ is low, a write into memory cycle is initiated. Once a memory cycle is initiated, $\overline{\text{WAIT}}$ is low and goes high when each cycle is completed.

When a memory read or write request is recognized by the address comparator and timing and control logic, the timing and control logic applies a Memory Request signal (MEM REQ) to the refresh logic to inhibit the start of any new memory refresh cycles. During a write cycle, the timing and control logic applies a Write Enable signal (READ/WRITE low) and RAM ENCLK to the 4K RAM. Simultaneously, the refresh logic applies an Address Select signal (ADDR SEL) to the address buffers and multiplexer to gate the memory address ($\overline{\text{ADDR0}}$ through $\overline{\text{ADDR11}}$) into RAM and data from the bus ($\overline{\text{BUS0}}$ through $\overline{\text{BUS7}}$) is written into the addressed memory space. During a read cycle, the operation is the same except the timing and control logic applies a Read Enable signal (READ/WRITE high) to the 4K RAM and a READ ENCLK to the bus drivers to gate the accessed eight-bit data byte (READ DATA) from memory onto the data bus.

The 4K RAM is a 4K by 8 array that requires periodic pseudo read cycles (memory locations accessed but data not released to the bus) to ensure that no data is lost from its internal data storage mechanisms. This function is accomplished in a cycle stealing fashion by reading one memory row (one address combination out of 64) every 32 microseconds when memory is not busy. When no other module is requesting a memory access and a read or write cycle is not in progress, a refresh cycle is initiated by the application of a high MEM REQ signal from the timing and control logic to the refresh logic. The high MEM REQ signal also causes the timing and control logic to apply a Read Enable signal (READ/WRITE high) to RAM. Once initiated, the refresh logic applies ADDR SEL to the address multiplexer which gates the first six-bit psuedo read address (PADDR) from the refresh logic address counter to RAM. Simultaneously, a Refresh In Progress signal (RFSH ON) from the refresh logic causes the timing and control logic to apply RAM ENCLK to RAM which refreshes the first memory location. The timing and control logic keeps accessed data off the bus by disabling the RAM bus drivers (READ ENCLK low). At the completion of each refresh cycle, the refresh logic address counter is incremented by one. After 32 microseconds, another refresh cycle is initiated and the next memory location is refreshed. MEM REQ remains high until a memory access is requested. Once a request is recognized by the address comparator and timing and control logic (ACS REQ high, $\overline{\text{I/O}}$ high, and $\overline{\text{REQ}}$ low), MEM REQ goes low and the refresh logic is inhibited from starting the next refresh cycle until MEM REQ again goes high.

2-27. INPUT/OUTPUT SECTION

The input/output section consists of a keyboard subsection, computer subsection, storage subsection, and peripheral subsection. Combined, these subsections provide data storage and retrieval capabilities and a complete communication link between the terminal and the terminal operator, an external central processing unit, and external peripheral equipment.

2-28. KEYBOARD SUBSECTION. The keyboard subsection provides the communication link between the terminal operator and the terminal. The process of recognizing data entry from the keyboard is accomplished by the control section Processor PCA. All the keyboard keys are arranged in a matrix of 14 columns of eight key switches each. This matrix is constantly monitored by the Processor PCA one column at a time. As each column is scanned, it appears to the Processor PCA as an eight-bit word where each bit represents one key switch in the column. Depressed keys are represented by a logic "1" and released keys by a logic "0". Because the key columns are monitored sequencially, the present state of each key must be compared to its previous state when last scanned in order for the Processor PCA to recognize when a key has just been depressed, is being held depressed, or has just been released. The previous state of each key is stored in the memory section and applied to the keyboard subsection one column byte (one bit for each key in the column) at a time. Each previous state byte corresponds to the matrix column being scanned and is applied to the subsection for comparison just before the column is read.

As shown in figure 2-2, the keyboard subsection consists of the Keyboard Interface PCA and the Keyboard Assembly. The Keyboard Interface PCA contains the bus decoder logic, an option jumper network, a speaker alarm generator, and input and output data buffers. The Processor PCA accesses the subsection by applying $\overline{\text{I/O}}$, $\overline{\text{REQ}}$, and the keyboard address ($\overline{\text{ADDR4}}$, and $\overline{\text{ADDR9}}$ through $\overline{\text{ADDR11}}$) to the bus decoder logic. $\overline{\text{ADDR0}}$ through $\overline{\text{ADDR3}}$ and $\overline{\text{ADDR5}}$ are instruction addresses that determine the keyboard function to be performed. The logic level of $\overline{\text{WRITE}}$ determines if data is to be received or transmitted by the keyboard. When $\overline{\text{WRITE}}$ is low, the bus decoder logic applies a Data Input Enable signal (DATA IN EN) to the input buffers and previous state column data and alarm instructions can be applied to the Keyboard Assembly.

When $\overline{\text{WRITE}}$ is high, the bus decoder logic applies a Data Output Enable signal (DATA OUT EN) to the output buffers and data from the subsection under control of the Processor PCA is applied back to the control and memory sections. Upon request from the Processor PCA ($\overline{\text{WRITE}}$ and $\overline{\text{ADDR0}}$ high and $\overline{\text{ADDR1}}$ through $\overline{\text{ADDR3}}$ low) the bus decoder logic applies a Read Jumper signal (RD JMPRS) to the option jumper network and an eight-bit data word defining the configuration of the operating option jumpers is applied through the output buffers onto the data bus. (A discussion of the jumper configurations is contained in section I of this manual.) The alarm generator is also under control of the processor PCA. Upon instruction ($\overline{\text{WRITE}}$ low and $\overline{\text{ADDR5}}$ and $\overline{\text{BUS7}}$ high), the bus decoder logic generates an Alarm Enable signal (ALARM.EN) that enables the alarm generator which activates the Keyboard Assembly speaker. Other instructions decoded and applied to the Keyboard Assembly include Column Output Enable ($\overline{\text{WRITE}}$ and $\overline{\text{ADDR5}}$ low), Light Emitting Diode Enable ($\overline{\text{WRITE}}$ low and $\overline{\text{ADDR5}}$ high), and Read Columns 0 through 14 ($\overline{\text{WRITE}}$ high and $\overline{\text{ADDR1}}$ through $\overline{\text{ADDR3}}$ low).

As shown in figure 2-2, the Keyboard Assembly contains LED, input, and output registers, data comm logic, a column decoder, ramp generator, 8 by 14 key matrix, differential comparators, and column byte buffers. The light emitting diode (LED) register is loaded with seven data bits (BUS0 through BUS6) and applies these bits (one bit for each LED) to the keyboard LEDs when the LED Enable signal (LED EN) is applied from the bus decoder logic. The input register holds column previous state data (BUS0 through BUS7) and applies this previous column byte (PBIT0 through PBIT7) to the reference voltage input of the differential comparators upon receipt of the Column Output Enable signal (COL OUT EN) from the bus decoder logic. This occurs just before each new column is scanned. The output register holds the newly scanned differentiated column byte from the differential comparators and releases the eight-bit byte (COL OUT) to the data bus upon receipt of RD·$\overline{\text{COL15}}$ from the bus decoder logic. The data comm logic contains a baud rate encoder and the keyboard data communication switches (BAUD RATE, DUPLEX, and PARITY) which generate a six-bit data comm byte (BD RATE/PAR/DPLX). Each time the 14 columns of the 8 by 14 key matrix have been scanned, the column decoder generates a Read Column 15 signal (RD·COL15) which releases the data comm byte to the data bus. (BUS1 through BUS3 define baud rate; BUS4 and BUS5 define parity; and BUS7 defines duplex.)

The column decoder, 8 by 14 key matrix, ramp generator, and differential comparators work in conjunction to generate the eight-bit scanned column byte (COL OUT) applied to the output register. When the Processor PCA issues instructions to read a column of the key matrix, the column decoder decodes the correct column address from ADDR0 through ADDR3 and applies the appropriate Column Select signal (COL SEL) to the key matrix. When RD·$\overline{\text{COL15}}$ goes high, the ramp generator is enabled and applies Drive Current (DR CUR) to the key matrix drive wires. Depressed keys in the selected column couple the drive wire signals to the sense wires which apply the signals (CBIT0 through CBIT7) to their respective differential comparators. As previously discussed, before a column is read, the previous state of that column is applied to the differential comparators by the Processor PCA through the input register. The differential comparators (one comparator for each row in the matrix) compare the previous and current state of each switch in the selected column and set corresponding bits in the output register. When RD·$\overline{\text{COL15}}$ from the bus decoder logic goes high, the eight-bit contents of the output register are gated through column byte buffers onto the data bus.

2-29. COMPUTER SUBSECTON. The computer subsection provides the communication link between the terminal and an external computer. The subsection consists of the Asynchronous Data Comm PCA and an interface cable assembly. The PCA transmits and receives bit serial data to and from the external computer through the interface cable assembly, provides parallel-to-serial and serial-to-parallel conversion, and transmits and receives bit parallel data to and from the terminal through the Backplane Assembly (data bus). The interface cable assembly determines if the terminal is to be connected directly to the computer or to data sets for remote communication with the computer through telephone lines.

As shown in figure 2-2, the Asynchronous Data Comm PCA contains RS-232-C receivers and drivers, bus decoder logic, a baud rate generator, control logic, and a universal asynchronous receiver/transmitter (UAR/T). The RS-232-C receivers and drivers provide the RS-232-C standard voltage interface for serial data transfers and interface control between the terminal and external computer. The drivers convert output signals from TTL levels (H= > 2.0V; L = < 0.8V) to RS-232-C levels (H = > +3.0V; L = < -3.0V). The receivers convert input signals from RS-232-C levels to TTL levels. There are six interface output signals. The Request To Send signal (CA) is generated by the control logic and is used when the terminal is connected to a data set to begin a transmit operation. The Data Terminal Ready signal (CD) is generated at the driver and is always true (high) as long as power is applied to the terminal. The Secondary Channel Transmit signal (SA) is generated by the control logic and is high unless a Break signal is generated. The Break signal is used by the terminal for remote interrupt to the computer and controls transmission of Serial Data Out (BA) from UAR/T. As long as $\overline{\text{BREAK}}$ is high, SA is high and BA can be transmitted from UAR/T. When $\overline{\text{BREAK}}$ is low, SA is low, the BA driver is disabled, and data cannot be transmitted to the computer. The remaining two interface outputs are TTL level clocks (EXT CLK OUT X8 and EXT CLK OUT X16) used only for special interface requirements. There are five interface input signals. The Serial Data In (BB) is applied directly to UAR/T. The Carrier Detect (CF), Clear To Send (CB), and Secondary Received Data (SB) are data set status signals and are applied directly to their respective terminal bus drivers. The remaining interface input is a TTL level clock (EXT CLK IN X16) used only for special interface requirements.

The processor accesses the subsection by applying $\overline{I/O}$, $\overline{REQ}$, and the PCA address ($\overline{ADDR9}$ through $\overline{ADDR11}$ high and $\overline{ADDR4}$ low) to the bus decoder logic. $\overline{ADDR5}$ and $\overline{ADDR6}$ are instruction addresses that determine the PCA function to be performed. The logic level of $\overline{WRITE}$ determines if data is to be received from or transmitted to the data bus. When $\overline{WRITE}$ is low, data is received from the data bus for transmission to the computer. When $\overline{WRITE}$ is high, data received from the computer is transmitted to the data bus. When $\overline{WRITE}$, $\overline{ADDR5}$, and $\overline{ADDR6}$ are low, the bus decoder logic generates a Transmit Strobe (XMIT STRB) which loads data from the bus (BUS0 through BUS7) into UAR/T. When $\overline{WRITE}$ and $\overline{ADDR5}$ are low and $\overline{ADDR6}$ is high, the bus decoder logic generates a low Control Load signal ($\overline{CNTL\ LD}$) which loads control data from the bus (BUS0 through BUS6) through the control logic register into UAR/T. When $\overline{WRITE}$ and $\overline{ADDR6}$ are high and $\overline{ADDR5}$ is low, the bus decoder logic generates a Status Enable signal (STAT EN) which gates seven status bits onto the data bus. When $\overline{WRITE}$, $\overline{ADDR5}$, and $\overline{ADDR6}$ are high, the bus decoder logic generates a Receive Reset signal which resets the UAR/T data received flag and, simultaneously, gates UAR/T data (DBIT0 through DBIT7) onto the data bus.

The baud rate generator defines bit timing during transmit/receive operations. Depending on the Baud Rate Select Code signals (BD RATE SEL) from the control logic, the baud rate generator generates one of eight baud rate clocks for the UAR/T (XMIT/RECEIVE CLK) and external computer (EXT CLK OUT X8 and EXT CLK OUT X16). Seven of the baud rates (110 to 9,600) are derived from the System Clock (SYS CLK) and one is derived from an external input (EXT CLK IN X16).

The control logic receives seven control bits (BUS0 through BUS6) from the bus and applies the bits to the baud rate generator, UAR/T, and RS-232-C drivers when $\overline{CNTL\ LD}$ is received from the bus decoder logic. BUS0 is the Request To Send bit ($\overline{CA}$) and is applied directly to its RS-232-C driver. BUS1 through BUS3 are the baud rate code bits (BD RATE SEL) applied to the baud rate generator. When the select code for 110 baud is detected, the control logic also applies a high 110 Baud signal (110 BD) to UAR/T indicating the need for two stop bits in the character format. For all other select codes, 110 BD is low indicating the format requirement of one stop bit. BUS4 and BUS5 are the Parity Select Code bits (PAR SEL) applied to UAR/T to select even, odd, or no parity. BUS6 is the interrupt bit and, when high, causes $\overline{SA}$ to go high and $\overline{BREAK}$ to go low disabling the data out RS-232-C driver.

The UAR/T is a full duplex device that can transmit and receive simultaneously. When transmitting to the computer, it receives parallel data (BUS0 through BUS7) from the data bus when XMIT STRB is applied. It converts the parallel data to serial information, appends the required asynchronous character formatting bits (start, stop, and parity) according to the inputs from the control logic (110 BD and PAR SEL), and transmits the information at the selected baud rate of XMIT/RECEIVE CLK from the baud rate generator. When transmitting to the terminal, UAR/T starts receiving serial data from the computer when it detects a valid start bit. It checks character parity, removes the start and stop bits, converts the data to parallel information, and transmits the information to the terminal bus. The UAR/T also generates four status outputs that indicate when it can receive parallel data from the data bus for transmission, when serial data has been received from the external computer, when a received character has incorrect parity, and when an overrun condition exists (UAR/T receive buffer full and a new character is loaded into it).

2-30. STORAGE SUBSECTION. The storage subsection consists of a CTU Interface PCA, a Read/Write PCA, a CTU Top Plane Assembly, two CTU Transport Assemblies, and tape cartridges.

2-31. CTU Interface PCA. The CTU Interface PCA provides the required interfacing between the storage subsection and basic terminal, decodes CTU operating instructions for the Read/Write PCA, encodes parallel binary data from the terminal into bi-phase coded serial data for the CTU's, and decodes bi-phase coded serial data from the CTU's into parallel binary data for the terminal. As shown in figure 2-2, the CTU Interface PCA basically consists of an address comparator, bus decoder and command logic, parallel-to-serial and serial-to-parallel conversion logic, data encoder/decoder logic, and CTU status logic.

The address comparator applies a low Address Enable signal ($\overline{ADDR}$) to the bus decoder and timing logic whenever a valid address from the terminal control section is recognized. $\overline{ADDR}$ is determined by the combination of the address jumpers (W1 through W4) configuration and four address bits ($\overline{ADDR4}$ and $\overline{ADDR9}$ through $\overline{ADDR11}$). In addition to a valid address ($\overline{ADDR}$), two control signals ($\overline{REQ}$ and $\overline{I/O}$) must also be low in order for the bus decoder and timing logic to decode function instructions from the control section. Depending on the logic levels of $\overline{ADDR5}$ and $\overline{WRITE}$, the bus decoder and timing logic generates the signals required to initiate one of four functional operations. When $\overline{ADDR5}$ and $\overline{WRITE}$ are both high, a read status operation is initiated. When $\overline{ADDR5}$ is high and $\overline{WRITE}$ is low, a write command operation is initiated. When $\overline{ADDR5}$ is low and $\overline{WRITE}$ is high, a read data operation is initiated. When $\overline{ADDR5}$ and $\overline{WRITE}$ are both low, a write data operation is initiated.

During a read status operation, the bus decoder and timing logic gates the current status of the storage subsection (SBIT0-SBIT7) through the status bus drivers onto the data bus ($\overline{BUS0}$-$\overline{BUS7}$) with a high Status Enable signal (STATUS EN). Status bits 0 and 1 indicate whether or not tape cartridges are inserted in Unit 0 and Unit 1 CTU Transport Assemblies, respectively. When tape cartridges are inserted, high Cartridge Inserted signals (CIN0 and CIN1) are applied to the drivers from the Read/Write PCA cartridge detect circuit. When the cartridges are removed, CIN0 and CIN1 go low. Status bit 2 indicates the presence

of CTU head current. Whenever recording gap, a high Record In Progress signal (RIP) is applied to the driver from the Read/Write PCA write current circuit. During read opeations, RIP is low. Status bit 3 indicates the tachometer-to-tape motion ratio (58.4 tachometer edges per inch tape motion divided by two) when either CTU Transport Assembly is in use. This signal is derived from the Tachometer Frequency signal (TACH) generated by the Read/Write PCA tachometer feedback circuit. TACH is clocked through the tachometer logic which divides TACH by two and applies it (1/2 TACH) to the status bus driver. A delayed version of 1/2 TACH (D1/2 TACH) is also applied to the tachometer flip-flop.

Status bit 4 indicates when a hole is detected in the selected CTU Transport Assembly tape. When a hole is detected, the selected CTU Transport Assembly applies a Hole Detected signal (NHOL0 or NHOL1) to the hole detect logic which generates a Hole Detect signal (HOL DET) to set the hole detect flip-flop. When set, the hole detect flip-flop applies a high HOLE signal to the driver. After status is read, the command logic applies a RESET signal to the flip-flop which causes the HOLE signal to go low. The hole detect logic enabling signal is the Unit Select 1 signal (US1) generated by the command logic. When US1 is high, the Unit 1 portion of the hole detect logic is enabled, the Unit 0 portion is disabled, and a low Unit Select 0 signal (US0) is generated to activate the Read/Write PCA Unit 1 circuits as discussed in paragraph 2-32. When US1 is low, the Unit 1 portion of the hole detect logic is disabled, the Unit 0 portion is enabled, and a high US0 is applied to the Read/Write PCA to activate its Unit 0 circuits. Status bit 5 indicates the output of the Read/Write PCA gap detect circuit (GAP) discussed in paragraph 2-32. GAP is normally high and goes low whenever the first eight bits of a preamble are detected. Status bit 6 is the Byte Ready signal (BYTE RDY) generated by the encoder/decoder logic. When high, BYTE RDY indicates that the data I/O buffer is ready to be loaded or unloaded. During write data operations, BYTE RDY is generated each time a data byte is decoded into bit serial data or whenever the end of a preamble is detected. Whenever the bus decoder and timing logic decodes a read or write data instruction, a Read Or Write signal (RD +WRT) is applied to the encoder/decoder logic which causes BYTE RDY to go low (reset). Status bit 7 is the INTERRUPT signal generated by a three-input "nand" gate. An interrupt condition occurs when a data byte is ready to be read or when a new byte of data is required for recording (BYTE RDY from encoder/decoder logic), during tachometer cycle edge transitions (D1/2 TACH from tachometer flip-flop), and during hole detect edge transitions (HOLE from the hole detect flip-flop). After status is read, the command logic generates a RESET signal to clear interrupts.

During a write command operation, the bus decoder and timing logic permits command data ($\overline{BUS0}$-$\overline{BUS7}$) to be loaded into the command logic by generating a negative-going Command Clock pulse (CMMD CLK). The command logic decodes $\overline{BUS0}$-$\overline{BUS7}$ into output commands that control the operation of the CTU Transport Assemblies. Command bits 0, 1, and 2 control cartridge tape motion. Bit 0 is the Servo Run command (SRUN) which is used in conjunction with a high NSTOP signal to generate $\overline{SRUN}$ required to enable the tape motion decoder. It should be noted that whenever a tape hole is detected, SRUN is disabled by DHOL DET from the hole detect logic which stops all tape motion. Depending on their logic levels, command bit 1 is used as a Forward or Reverse command (FWD/REV) for the tape motion decoder and bit 2 is used as a Fast or Slow command (FAST/SLOW). When enabled, the tape motion decoder combines these run commands and generates one of four CTU run commands; Fast Forward (NFFD), Slow Forward (NSFD), Fast Reverse (NFREV), or Slow Reverse (NSREV). The generated run command is applied to the Read/Write PCA CTU drive circuits as discussed in paragraph 2-32. The command logic also combines command bits 0, 1, and 2 to generate an Interface Slow Forward command (NISF) which is used by the encoder/decoder logic to prevent discontinuity in encoded or decoded data when a cartridge tape hole is detected.

Command bit 3 is used to generate Record Enable commands (RE and NRE) that are applied to the encoder/decoder logic to specify a read or write function. NRE is also applied to the Read/Write PCA write current circuit and unit/function decoder as discussed in paragraph 2-32. When RE is low (NRE high), a read function is specified which enables the decoder portion of the encoder/decoder logic. When RE is high (NRE low), a write function is specified and the encoder logic is enabled. Bit 4 is the US1 signal for the hole detect logic as previously discussed. Bit 5 is the Record Gap command (REC GAP) which is applied to the encoder portion of the encoder/decoder logic during a write data function to specify a record gap. Bits 6 and 7 are the Light Unit 1 (NL1) and Light Unit 0 (NL0) commands respectively. NL1 and NL0 are applied to the CTU Transport Assemblies to light the eject button indicator lamps as discussed in paragraph 2-33.

During a read data operation (RE low), the data to be read is applied to the decoder portion of the encoder/decoder logic in a bi-phase coded serial bit stream (NDZX) from the Read/Write PCA read amplifier circuit as discussed in paragraph 2-32. At the appropriate time, the encoder/decoder logic generates a high Shift 0 signal (S0) and low Shift 1 signal (S1) which enables the shift register to accept bit serial data and shifts the first seven bits of delayed NDZX (RD DATA) into the shift register. The data I/O buffer is set to accept an input data byte from the shift register and encoder/decoder logic by a high Read/Write Select signal (RD/WRT SEL) from the bus decoder and timing logic and, once the seven bits of RD DATA are in the shift register, the register contents (BIT0-BIT6) are parallel-loaded into the data I/O buffer along with the eighth data bit (BIT7) from the decoder logic. The 8-bit data byte is then clocked out of the data I/O buffer as a parallel byte (DBIT0-DBIT7). DBIT0-DBIT7 is gated through the data bus drivers and onto the terminal's data bus ($\overline{BUS0}$-$\overline{BUS7}$) by a high Read Enable signal (READ EN) from the bus decoder and timing logic.

During a record data operation (RE high), the bus decoder and timing logic applies a low RD/WRT SEL signal to the data I/O buffer which sets the buffer to accept parallel input data ($\overline{BUS0}$-$\overline{BUS7}$) from the terminal's data bus. At the appropriate time, the encoder/decoder logic generates high S0 and S1 signals which enable the shift register to accept parallel input data and DBIT0-DBIT7 is clocked out of the data I/O buffer into the shift register. When S1 goes low, DBIT0-DBIT7 are shifted out of the register in a serial bit stream (REC DATA) and applied to the encoder portion of the encoder/decoder logic. The encoder converts the bit serial data into bi-phase coded serial data (NDATA) which is applied to the Read/Write PCA unit/function decoder as discussed in paragraph 2-32.

2-32. Read/Write PCA. The Read/Write PCA, under control of the CTU Interface PCA, selectively operates one of the two CTU Transport Assemblies. Basically, the Read/Write PCA consists of CTU drive and feedback circuits, read/write circuits, and CTU select circuits. As shown in figure 2-2, CTU run commands (NFFD, NSFD, NFREV, and NSREV) are applied to the CTU drive circuits from the CTU Interface PCA. When any of these signal levels go low, the drive circuits apply a corresponding Drive signal (0 DRIVE or 1 DRIVE) to the selected CTU Transport Assembly to drive the tape at the selected speed and in the selected direction. The CTU drive circuits consist of a command ramp circuit, a threshold detect circuit, and a power amplifier circuit. The command ramp circuit converts the run commands into corresponding ramped command voltages that are changed into ramped command currents and applied to the power amplifier's current summing junction along with tachometer feedback current. The ramp voltage levels determine tape speed (±1.2 volts = ±10 ips; ±7.2 volts = 60 ips) and the voltage polarity determines tape direction (+ = forward; – = reverse). When the ramp voltage reaches a level indicating a minimum tape speed of ±1.0 ips, the threshold detect circuit generates a Running signal (RUNG) required to enable the amplifier select logic. Simultaneously, depending on the polarity of the detected ramp voltage, the threshold detect circuit applies one of two Feedback Enable signals (FDBK EN) to the feedback circuits which enables the appropriate tachometer feedback circuit. The power amplifier circuit consists of two identical power amplifiers that alternately share a common current summing junction. Under control of the two Amplifier Select signals (0/1 AMP SEL) from the amplifier select logic, the selected amplifier input is switched to the current summing junction and generates the appropriate dirve signal for the selected CTU Transport Assembly. Simultaneously, the unused amplifier is switched to a low gain mode to inhibit the remaining CTU Transport Assembly by switching off a local feedback shunt switch.

When RUNG is high, Unit Select 0 signal (US0) from the CTU Interface PCA is high, and Unit 0 Cartridge Inserted signal (CIN0) from the cartridge detect circuit is high, the amplifier select logic applies a low 0 SEL signal to the CTU drive circuits which enables the power amplifier for Unit 0 CTU Transport Assembly. When US0 is low, Unit 1 Cartridge Inserted signal (CIN1) is high and RUNG is high, a low 1 SEL signal enables the power amplifier for Unit 1 CTU Transport Assembly. High CIN0 or CIN1 signals are generated by the cartridge detect circuit whenever low 0NCI or 1NCI signals are received from the respective CTU Transport Assemblies as discussed in paragraph 2-33. From the previous discussion then, it should be noted that three conditions must exist before a CTU Transport Assembly can be driven; a unit select signal must be received, a run command must be received, and a tape cartridge must be installed in the selected CTU Transport Assembly (CIN0 or CIN1).

When running, the selected CTU Transport Assembly's tachometer generates a sine wave frequency (T) proportional to the driven tape speed which is applied to the tachometer feedback select and conditioning circuits. The tachometer feedback select and conditioning circuits detect and convert T into a TTL level signal and, depending on the logic level of US0, gate the selected Tachometer Feedback Frequency (TACH FREQ) to the feedback circuits. Simultaneously, TACH FREQ is delayed and inverted and this signal (TACH) is applied to the CTU Interface PCA (paragraph 2-31) and to the feedback circuits along with TACH FREQ. TACH and TACH FREQ are gated through doubling logic in the feedback circuits to generate a Twice Tachometer Frequency signal (2XTACH) which drives a one-shot multivibrator in the feedback circuits. The output of the one-shot is applied to two OR gates and, depending on the polarity of the ramp voltage as previously discussed, is gated into one of two feedback circuits by FDBK EN. The generated feedback voltage is changed into Feedback Current (FDBK) and applied back to the power amplifier's current summing junction in the CTU drive circuits.

The read/write circuits consist of a unit/function decoder, read select switch, read amplifier circuit, write current circuit, and a gap detect circuit. Record Enable (NRE), US0, and bi-phase coded Write Data (NDATA) are applied to the unit/function decoder from the CTU Interface PCA as discussed in paragraph 2-31. The unit/function decoder decodes the logic levels of US0 and NRE into CTU Transport Assembly unit select signals and into read or write functions. When NRE and US0 are high, the decoder applies a high Unit 0 Read Select signal (0 RD SEL) and a low Unit 1 Read Select signal (1 RD SEL) to the read select switch which simultaneously disables the unit 1 section of the switch and allows data from the Unit 0 CTU Transport Assembly (0 RD DATA) to pass through the switch to the read amplifier circuit. When NRE is high and US0 is low, 0 RD SEL goes low and 1 RD SEL goes high which disables the unit 0 section of the switch and allows data from Unit 1 CTU Transport Assembly (1 RD DATA) to be applied to the read amplifier circuit. When NRE and US0 are low, 0 RD SEL and 1 RD SEL are low which disables the read select switch and NDATA is toggled through the unit/function decoder (1 WRT DATA) to Unit 1 CTU Transport Assembly. The WRT DATA is a bi-phase serial bit stream and is applied to the CTU read/write head on the HEAD + and HEAD – lines. High levels of the bit stream cause the read/write head to write flux in a north seeking pole direction and low levels write flux in a south seeking pole direction. When NRE is low and US0 is high, the read select switch is disabled (0 and 1 RD SEL both low) and NDATA

is applied to Unit 0 CTU Transport Assembly (0 WRT DATA). NRE is also applied to the write current circuit and, when low, enables the circuit to generate the Head Current (HEAD CT) required by the selected CTU Transport Assembly to record WRT DATA on the tape. Once enabled, the write current circuit also applies a high Record In Progress signal (RIP) to the CTU Interface PCA as discussed in paragraph 2-31. During read operations, NRE is high which disables the write current circuit.

During read operations, RD DATA from the selected CTU Transport Assembly is applied through the read select switch HEAD + and HEAD – lines to the read amplifier circuit. The read amplifier circuit amplifies and detects these signals, generates the TTL level bi-phase coded serial bit stream (NDZX), and applies detected data flux reversals (FLX REV) to the gap detect circuit. The gap detect circuit monitors the presence of flux reversals. After eight flux reversals at 8000 Hz (10 ips) are detected (preamble for valid data), the gap detect circuit generates a low GAP signal. The low GAP signal gates NDZX from the read amplifier circuit to the CTU Interface PCA as discussed in paragraph 2-31. GAP will remain low until no flux reversals are detected for more than eight bit times which indicates a recorded gap area. When a gap area is detected, GAP goes high and remains high until another preamble is detected. The high GAP signal holds the NDZX line to the CTU Interface PCA high to blank out any noise generated by the read amplifier citcuit.

2-33. CTU Transport Assembly. The terminal contains two identical tape transport assemblies (Unit 0 and Unit 1) each consisting of a CTU Base Assembly, a Motor/Tachometer Assembly, and a Head Bridge Assembly. Since the units are identical, only one will be discussed. Refer to paragraphs 2-31 and 2-32 for unit selection discussion. The CTU Base Assembly provides the tape cartridge load and eject mechanisms and the Motor/Tachometer Assembly provides the tape motion mechanisms. The Head Bridge Assembly consists of the read/write head and CTU Electronics PCA. The CTU Electronics PCA provides connections for read/write head signals (HEAD +, HEAD –, HEAD GND, and HEAD CT) and tachometer signals (T, TCOM, and TGND) discussed in paragraph 2-32 and contains the unit select lamp circuit and hole detection circuit. In addition, the PCA also contains two mechanically activated switches S1 and S2. When a tape cartridge is inserted into the transport assembly, S2 is closed and a low Cartridge Inserted signal (NCI) is applied to the Read/Write PCA as discussed in paragraph 2-32. Switch S1 is a normally closed switch. When a tape cartridge is inserted into the transport assembly with its RECORD tab either removed or not set to the record position, S1 is opened and the Head Write Current (HEAD CT) circuit between the read/write head and the Read/Write PCA is disabled.

The CTU Electronics PCA lamp circuit applies +5V across unit select indicator lamp DS1 whenever a low Lamp signal (NL) is received from the CTU Interface PCA as discussed in paragraph 2-31. The hole detection circuit consists basically of an infrared emitting diode, a phototrahsistor, and a one-shot multivibrator. Usually, the diode irradiance is blocked by the opaqueness of the magnetic tape. However, when Beginning-Of-Tape, Load Point, Early Warning, or End-Of-Tape holes pass over the diode, the irradiance passes through the holes and activates the phototransistor which in turn triggers the one-shot. Each time it is triggered, the one-shot generates a Hole Detect signal (NHOL) for the CTU Interface PCA as discussed in paragraph 2-31.

2-34. PERIPHERAL SUBSECTION. The peripheral subsection provides the communication link between the terminal and an associated external peripheral device. The subsection consists of the Terminal Duplex Register PCA and an interface cable assembly. The PCA is a general purpose, parallel input/parallel output, interface device that provides eight data outputs, input/output commands, and an external strobe for its associated peripheral. The PCA accepts eight data inputs, input/output control-in, and eight status inputs from the peripheral. Data and instructions from the terminal are applied to the PCA through the Backplane Assembly (data bus). Communication between the PCA and external peripheral is provided by an interface cable assembly that is compatible with both the PCA edge connector and selected external peripheral. (A 9866 Cable Assembly is currently available from Hewlett-Packard to interface between the PCA and an HP 9866A Printer.)

As shown in figure 2-2, the Terminal Duplex Register PCA contains an address comparator, bus decoder logic, a strobe generator, control logic, an input register, and an output register. In addition, the PCA contains 15 jumper options that provide the user with the means to configure the PCA as required for specific interface requirements. Table 2-1 contains a list of the jumpers and a definition of each jumper function.

The address comparator applies an Address Enable signal (ADDR) to the bus decoder logic whenever a valid module address from the control section is recognized. ADDR is determined by the combination of the address jumper configuration (table 2-1) and four address bits ($\overline{\text{ADDR4}}$ and $\overline{\text{ADDR9}}$ through $\overline{\text{ADDR11}}$). The remaining address bits ($\overline{\text{ADDR0}}$ through $\overline{\text{ADDR2}}$) are instruction addresses and are applied to the bus decoder logic along with three address control signals ($\overline{\text{REQ}}$, $\overline{\text{I/O}}$, and $\overline{\text{WRITE}}$) to determine the Terminal Duplex Register PCA function to be performed. In addition to the correct address, both $\overline{\text{REQ}}$ and $\overline{\text{I/O}}$ must be low in order for the bus decoder logic to decode function instructions from the control section. Depending on the combined logic levels of $\overline{\text{ADDR0}}$, $\overline{\text{ADDR1}}$, $\overline{\text{ADDR2}}$, and $\overline{\text{WRITE}}$, the bus decoder logic generates one of nine output signals that initiate the execution of received control section instructions. The instruction codes and the resulting bus decoder logic output signals are listed in table 2-2. When triggered by PULSE OUT from the bus decoder logic, the strobe generator generates a buffered one-microsecond pulse for the external peripheral. The polarity of the pulse is determined by strobe jumpers P and Q as discussed in table 2-1.

The control logic consists of a Command Out flip-flop, Command In flip-flop, and associated logic circuits and

Table 2-1. Terminal Duplex Register PCA Jumper Options

JUMPER	FUNCTION
A, B	Jumpers A and B are used to tie the input registers eight data input bias resistors to either +5V or ground. When jumper B is installed, the resistors are tied to +5V. When jumper A is installed, the resistors are tied to ground. Jumpers A and B *cannot* be installed at the same time. If both jumpers are installed, a short between +5V and ground is created.
C	When jumper C is installed, the control logic Command Out flip-flop is set (Command Out signal true) each time output data is clocked into the output register. (Refer to jumper M.) When jumper C is removed, the Command Out flip-flop is set only when the bus decoder logic decodes the appropriate I/O instruction.
D	Not used.
E–H	Jumpers E through H correspond to $\overline{\text{ADDR4}}$, $\overline{\text{ADDR9}}$, $\overline{\text{ADDR10}}$, and $\overline{\text{ADDR11}}$, respectively, and are used to select the address to which the PCA will respond. (For 9866 Printer interface addressing jumper F should be installed and jumpers E, G, and H removed.
J, K	Jumpers J and K are used to select the polarity of the Device In (jumper J) and Device Out (jumper K) signals that will reset the control logic Command In and Command Out flip-flops. When the jumpers are installed, the flip-flops will be reset by low Device In/Out signals. When the jumpers are removed, the flip-flops will be reset by high Device In/Out signals.
L, M	Jumpers L and M are used to select the polarity of the Command In (jumper L) and Command Out (jumper M) signals when their respective flip-flops are set. When the jumpers are installed, the Command In/Out signals are high when their flip-flops are set. When the jumpers are removed, the Command In/Out signals are low when the flip flops are set.
N	Jumper N controls the output registers eight data output buffers. When jumper N is removed, the output buffers are always enabled and data from the output register is inverted as it is applied to the external peripheral. When jumper N is installed, the output buffers are enabled only when the control logic Command Out flip-flop is set. When the jumper is installed and the flip-flop is reset, the outputs from the buffers are always high.
P–R	Jumpers P, Q, and R are used to select the Strobe signal applied to the external peripheral. When jumpers P or Q are installed, a one microsecond pulse is applied to the peripheral when the bus decoder logic decodes the appropriate I/O instruction. When jumper P is installed, a positive pulse is generated and, when jumper Q is installed, a negative pulse is generated. When jumper R is installed, the Strobe signal is always +5V. When no jumpers are installed, the Strobe signal line is open. Only one of jumpers P, Q, and R can be installed at the same time. If more than one jumper is installed, the strobe generator circuits may be damaged.

jumper networks. Both flip-flops are enabled by SYS CLK and both are configured so that if a conflict occurs between an instruction to set the flip-flop and an instruction to reset the flip-flop, the set instruction will always take precedence. The Command Out flip-flop can be set by either SET OUT FF from the bus decoder logic or by $\overline{\text{OUTPUT}}$ if jumper C (table 2-1) is installed. When set, the flip-flop generates a true Command Out signal (table 2-1, jumper M) for the external peripheral and, if jumper N (table 2-1) is installed, applies an Output Enable signal (OUTPUT EN) to the data output buffers. The flip-flop can be reset by either RESET OUT FF from the bus decoder logic or a Device Out signal (table 2-1, jumper K) from the external peripheral.

When set by SET IN FF from the bus decoder logic, the Command In flip-flop generates a true Command In signal (table 2-1, jumper L) for the external peripheral and simultaneously clocks input data ($\overline{\text{DBIT0}}$ through $\overline{\text{DBIT7}}$) into the input register with DATA IN CLK. The flip-flop can be

Table 2-2. Bus Decoder Logic Instruction Codes

INPUT SIGNAL AND LOGIC LEVEL				OUTPUT SIGNAL
$\overline{\text{WRITE}}$	$\overline{\text{ADDR2}}$	$\overline{\text{ADDR1}}$	$\overline{\text{ADDR0}}$	
L	H/L	H/L	H/L	$\overline{\text{OUTPUT}}$
H	H	H	H	$\overline{\text{INPUT STATUS}}$
H	H	H	L	$\overline{\text{INPUT DATA}}$
H	H	L	H	PULSE OUT
H	H	L	L	CMD FF STATUS
H	L	H	H	RESET OUT FF
H	L	H	L	RESET IN FF
H	L	L	H	SET OUT FF
H	L	L	L	SET IN FF

H = High
L = Low

reset by either RESET IN FF from the bus decoder logic or a Device In signal (table 2-1, jumper J) from the external peripheral. The status of the Command Out and Command In flip-flops (OUT FF STATUS and IN FF STATUS) are applied to the terminals data bus ($\overline{\text{BUS0}}$ and $\overline{\text{BUS7}}$ respectively) whenever CMD FF STATUS is decoded by the bus decoder logic and applied to the control logic.

As previously discussed, parallel data from the external peripheral ($\overline{\text{DBIT0}}$ through $\overline{\text{DBIT7}}$) is clocked into the input register with DATA IN CLK from the control logic. The input register inverts the data and applies it through the input buffers onto the data bus whenever the buffers are enabled by an Input Enable signal (INPUT EN) which is derived from the bus decoder logic $\overline{\text{INPUT DATA}}$ signal. Parallel data from the terminal ($\overline{\text{BUS0}}$ through $\overline{\text{BUS7}}$) is clocked into the output register with a Data Out Clock signal (DATA OUT CLK) which is derived from the bus decoder logic $\overline{\text{OUTPUT}}$ signal. The output register inverts the data and applies it through the output buffers to the external peripheral whenever the buffers are enabled (table 2-1, jumper N). Eight status inputs ($\overline{\text{SBIT0}}$ through $\overline{\text{SBIT7}}$) from the external peripheral can be gated onto the data bus by applying a Status Enable signal (STATUS EN) to the eight status input buffers. STATUS EN is generated whenever $\overline{\text{INPUT STATUS}}$ is decoded by the bus decoder logic. It should be noted that two of the status bits ($\overline{\text{SBIT0}}$ and $\overline{\text{SBIT1}}$) are inverted before they are applied to their respective input buffers.

CONTROL SECTION

PROCESSOR PCA

PRIOR IN
BUSY
DATA OUT
DATA REGISTER
UBCL
STROBE
UPPER BYTE ADDRESS REGISTER
I/O, WRITE, ADDR8 - ADDR13
BUS0-BUS7
BI10 - BIT7
BIT0 - BIT7
BIT6, BIT7
LOWER BYTE ADDRESS REGISTER
ADDR0 - ADDR7
DATA IN STROBE
BUS0,2,5,6, BUS7
LBCL
PRIOR IN
PRIOR OUT
RESTART/ LOAD
MICRO-PROCESSOR
STATUS
CYCLE DECODER
ENABLE
RESTART
BUS CYCLE LOGIC
REQ
BUS0, BUS2
INT
T2
T11
ø11
ø12
ATT
RESTART
RESTART LOGIC
ø12
PCL
RDY
SYNC
SYS CLK
CLOCK GENERATOR
ø12
ø11
RESTART
ø12
INTERRUPT GENERATOR
T11
RESTART
RUN
RUN

ROM PCA

SYS CLK
REQ
I/O
WRITE
TIMING AND CONTROL LOGIC
WAIT
OUT EN
READ ADDR
WAIT
ENABLE
10-12K SEL
8-10K SEL
6-8K SEL
4-6K SEL
2-4K SEL
0-2K SEL
12K ROM
ROM DATA
BUS0 - BUS7
ROM SELECT DECODER
ADDR11 - ADDR13
ADDR14, ADDR15
ADDRESS COMPARATOR
ADDR
STARTING ADDRESS JUMPERS
ADDR0 - ADDR10

P/O INPUT/OUTPUT SECTION

KEYBOARD SUBSECTION

KEYBOARD PCA

ADDR0 - ADDR3
COLUMN DECODER
DATA COMM LOGIC
BD RATE/ PAR/DPLX
DATA COMM BUFFERS
COL SEL
RD-COL15
RAMP GENERATOR
DR CUR
8 x 14 KEY MATRIX
CBIT0 - CBIT7
RD-COL15

KEYBOARD INTERFACE PCA

ADDR0 - ADDR3
RD-COL15
DIFFERENTIAL COMPARATORS
COL OUT
OUTPUT REGISTER
COLUMN BYTE BUFFERS
OPTION JUMPER NETWORK
PBIT0 - PBIT7
WRITE
REQ
I/O
BUS DECODER LOGIC
RD JMPRS
COL OUT EN
LED EN
ALARM EN
DATA IN EN
DATA OUT EN
ADDR0 - ADDR5 AND ADDR9 - ADDR11
INPUT REGISTER
BUS0 - BUS7
LED REGISTER
TO LEDS
INPUT BUFFERS
OUTPUT BUFFERS
BUS0 - BUS7
ALARM GENERATOR
BEEP
TO SPEAKER
DATA IN EN
DATA OUT EN

FROM CTU INTERFACE PCA
NDATA
US0
NRE
NFFD
NSFO
NFREV
NSREV
ADDR4, ADDR9 - ADDR11
SYS CLK
WRITE
ADDR5
I/O
REQ
BUS0 - BUS7
INTERRUPT

POWER SUPPLY SECTION

115V-230V PRIMARY POWER
POWER SUPPLY PCA
-42V
+12V
+5V
TO SWEEP PCA
+12V
-12V
+5V
TO BACKPLANE ASSY
SENSE
BASE DRIVE
POWER SUPPLY CONTROL PCA
LOGIC RESET
SYS CLK
+5V

MEMORY SECTION

+4K MEMORY PCA

WAIT
WAIT
WRITE
I/O
REQ
SYS CLK
TIMING AND CONTROL LOGIC
READ EN
RAM ENCLK
READ/WRITE
4K RAM
READ DATA
WRITE DATA
BUS0 - BUS7
MEM REQ
RFSH ON
REFRESH LOGIC
ADDR SEL
PADDR
ACS REQ
ADDRESS MULTIPLEXER
ADDRESS BUFFERS
ADDR12 - ADDR15
ADDRESS COMPARATOR
STARTING ADDRESS JUMPERS
ADDR0 - ADDR7
ADDR8 - ADDR11

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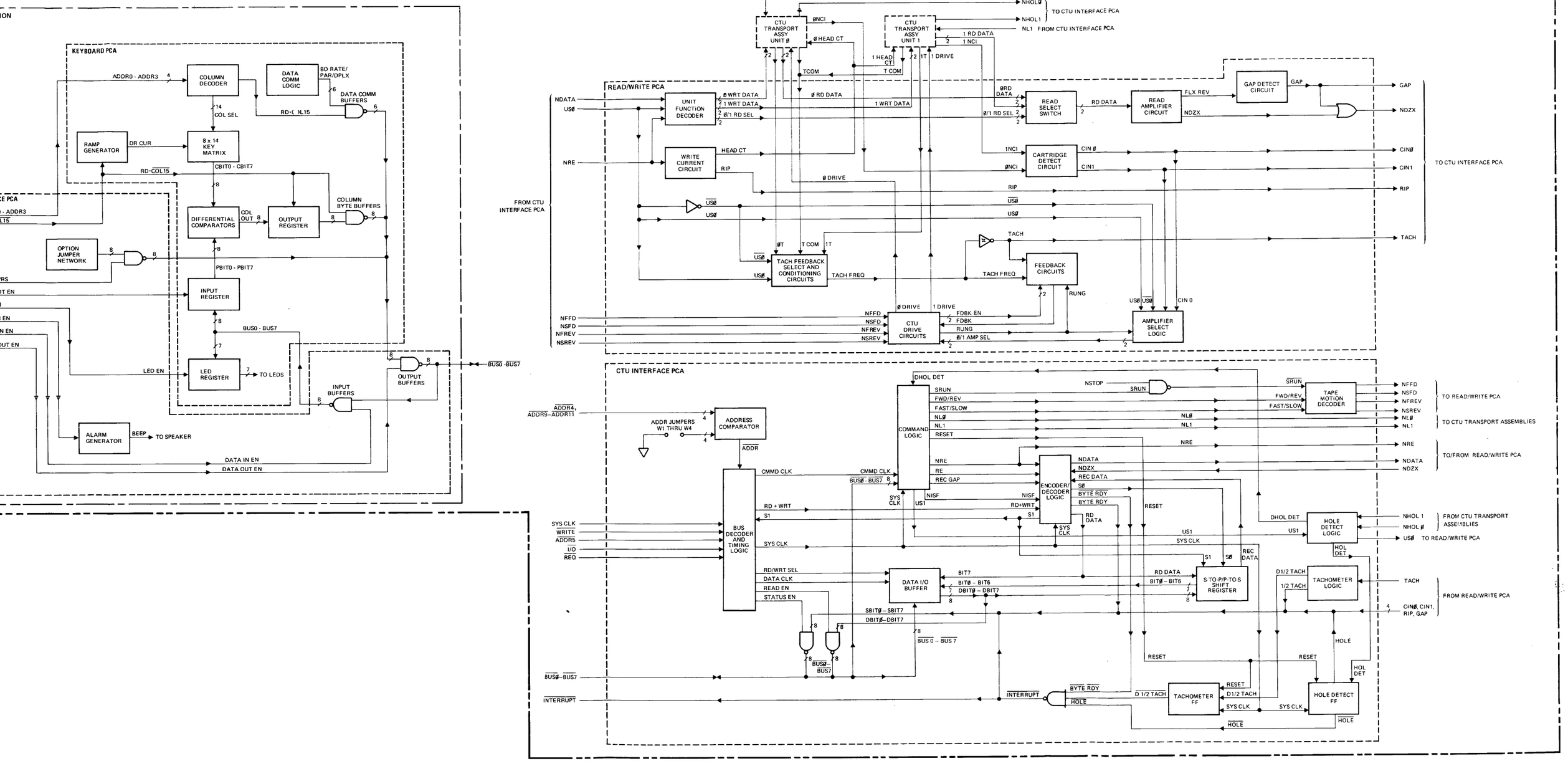

Figure 2-2. Detailed Block Diagram (Sheet 1 of 2)

DISPLAY SECTION

DISPLAY CONTROLLER SUBSECTION

P/O DISPLAY TIMING PCA

DISPLAY CONTROLLER CLOCK

CLK

DOT GENERATOR

D0

104-COLUMN COUNTER

N103

HORIZONTAL COLUMN BITS

TO CURSOR "X" COMPARATOR

TO DISPLAY EXPANSION PCA

TO CURSOR GENERATOR

P/O DISPLAY TIMING PCA

DISPLAY CONTROL PCA

D0, D0, D8, D8

D1

D2, D6, D8

DOT SHIFT GENERATOR

TO REFRESH LOGIC

P/O VIDEO LOGIC

N103

NHDR

TO SWEEP PCA

VRTCLK

HBLANK

TO DISPLAY EXPANSION PCA

TO VIDEO GENERATOR LOGIC

N81 PCA

0CIRC

0CIRCEN

TO REFRESH LOGIC

BUFCLK TO VIDEO GENERATOR LOGIC & ENHANCEMENT GENERATOR

FROM PROM CHARACTER PCA

DBIT0

SHFT CLK

D0, D8

LC0 - LC3 FROM SCAN LINE COUNTER

TO DISPLAY EXPANSION PCA

D8

UC/LC SELECT

CHARACTER SELECT LOGIC

NE1

CHARACTER GENERATOR ROMS

LSB

MSB

BIT 0 BIT4, BIT6

PARALLEL TO SERIAL CONVERTER

NBITS TO VIDEO GENERATOR LOGIC

NBIT0 - NBIT6 FROM DMA PCA

BIT5, BIT6

SET SELECT (NBSS0, NBSS1)

FROM DISPLAY EXPANSION PCA

NSET0 NBSSS0, NBSS1 NE1 BIT0 - BIT6 DBIT1 - DBIT7 FROM PROM CHARACTER PCA

TO PROM CHARACTER PCA

TO DMA PCA

VRTCLK

SCAN LINE COUNTER

N14

LC0 - LC3

25-ROW COUNTER

ROW COUNT

NIO3

P/O VIDEO LOGIC

GVS

VDR

TO SWEEP PCA

INTSET EVEN

VBLNK

TO DMA AND DISPLAY EXPANSION PCAS

TO CHARACTER GENERATOR AND PROM CHARACTER PCA

CURSOR LINE ENABLE LOGIC

L11

CLEN

N14

TO DISPLAY EXPANSION PCA

CURSOR "Y" COMPARATOR

CYEN

"Y" POSITION HOLDING REGISTER

"Y" POSITION

NBLNK

TO VIDEO GENERATOR LOGIC

NCYS

TO DMA PCA

BUS0 BUS4, BUS7

ADDR4, ADDR5, ADDR9 - ADDR11

WRITE

I/O

REQ

BUS DECODER NETWORK

NCYS NCXS

P/O DISPLAY TIMING PCA

FROM DISPLAY EXPANSION PCA

NXBITS 1

NBBL

NBUL

FROM VIDEO LOGIC

HBLANK

VIDEO GENERATOR LOGIC

VIDEO

IV

BLINK GENERATOR

BLINK

CBL

5 Hz

12 COUNTER

NCYS

NCXS

VBLNK

NBLNK

L11

NBITS

FROM "Y" POSITION HOLDING REGISTER

FROM PARALLEL TO SERIAL CONVERTER

INVERSE VIDEO FF

NIV

CLEN

VCSR

CURSOR GENERATOR

D0

FROM DOT GENERATOR

FROM VIDEO LOGIC

BUFCLK

FROM DMA PCA

CXEN

CURSOR "X" COMPARATOR

HORIZONTAL COLUMN BITS

FROM 104-COLUMN COUNTER

"X" POSITION HOLDING REGISTER

"X" POSITION

BUS0 BUS6

SWEEP PCA

HALF BRIGHT

HEIGHT

NHDR

FROM VIDEO LOGIC

WIDTH

DMA PCA

ADDR0-ADDR7

ADDR8-ADDR13

LOWER BYTE ADDRESS REGISTER

GVS

UPPER BYTE ADDRESS REGISTER

LINK

EOL+EOP

BUS0 - BUS7

HOLDING REGISTERS

CLOCK

INT SET

FROM DISPLAY CONTROL PCA

80-CHARACTER COUNTER

80

BUS CYCLE LOGIC

SYS CLK

PRIOR IN

PRIOR OUT

TO PROCESSOR PCA BUSY

TO CONTROL STORE PCA REQ

FROM CONTROL STORE PCA WAIT

ON/OFF

BUS6

DMA FF

FROM DISPLAY CONTROL PCA NCYS

DISPLAY FUNCTION PRIORITY ENCODER

FUNCTION CODE

INVERSE VIDEO FF

NIV

LB LOAD

DISPLAY FUNCTION DECODER

CONTROL

CHARACTER

EOP

EOL

LINK

DISPLAY FUNCTION LOGIC

L8LOAD

LOAD

EOL + EOP

EVEN ROW SHIFT REGISTER

EVEN ROW CLK

ODD ROW SHIFT REGISTER

ODD ROW CLK

EVEN

LINE BUFFERS

D1

TO DISPLAY TIMING PCA

FROM DISPLAY CONTROL PCA

REFRESH LOGIC

0CIRC

0CIRCEN

LOAD

NBIT0 - NBIT6

TO DISPLAY CONTROL PCA

DISPLAY EXPANSION PCA

BIT0 BIT4, BIT6

TO PROM CHARACTER PCA

CHARACTER SELECT LOGIC

SELECT 64/128

64/128 CHARACTER SET 1

64/128 CHARACTER SET 2

64/128 CHARACTER SET 3

MSB

SEN

SN

LSB

FROM DISPLAY TIMING PCA

VRTCK

SCAN LINE COUNTER

N14

LC0 LC3

DBIT0 - DBIT8

DBIT1 - DBIT7

FROM DISPLAY CONTROL PCA

REFRESH AND LOAD LOGIC

BSEL

CHARACTER SET ENCODER

1SEN 2SEN 3SEN

SHIFT ENABLE

LOAD

LBLOAD

HOLDING REGISTER

INT SET

FROM DISPLAY CONTROL PCA

BUS0, BUS2 BUS5

LINE BUFFERS

NBSS0

NBSS1

CHARACTER SET DECODER

SHIFTER LOGIC

DBIT0, DBIT8

SHFT CLK

CLK

FIELD

TO DISPLAY CONTROL AND PROM CHARACTER PCAS

FROM DISPLAY TIMING PCA

ULEN

HBEN

BLEN

ENHANCEMENT GENERATOR

NBHB TO SWEEP PCA

NBBL

NBUL

TO DISPLAY TIMING PCA

0CIRC

NB1

BUFCLK

FROM DISPLAY TIMING PCA

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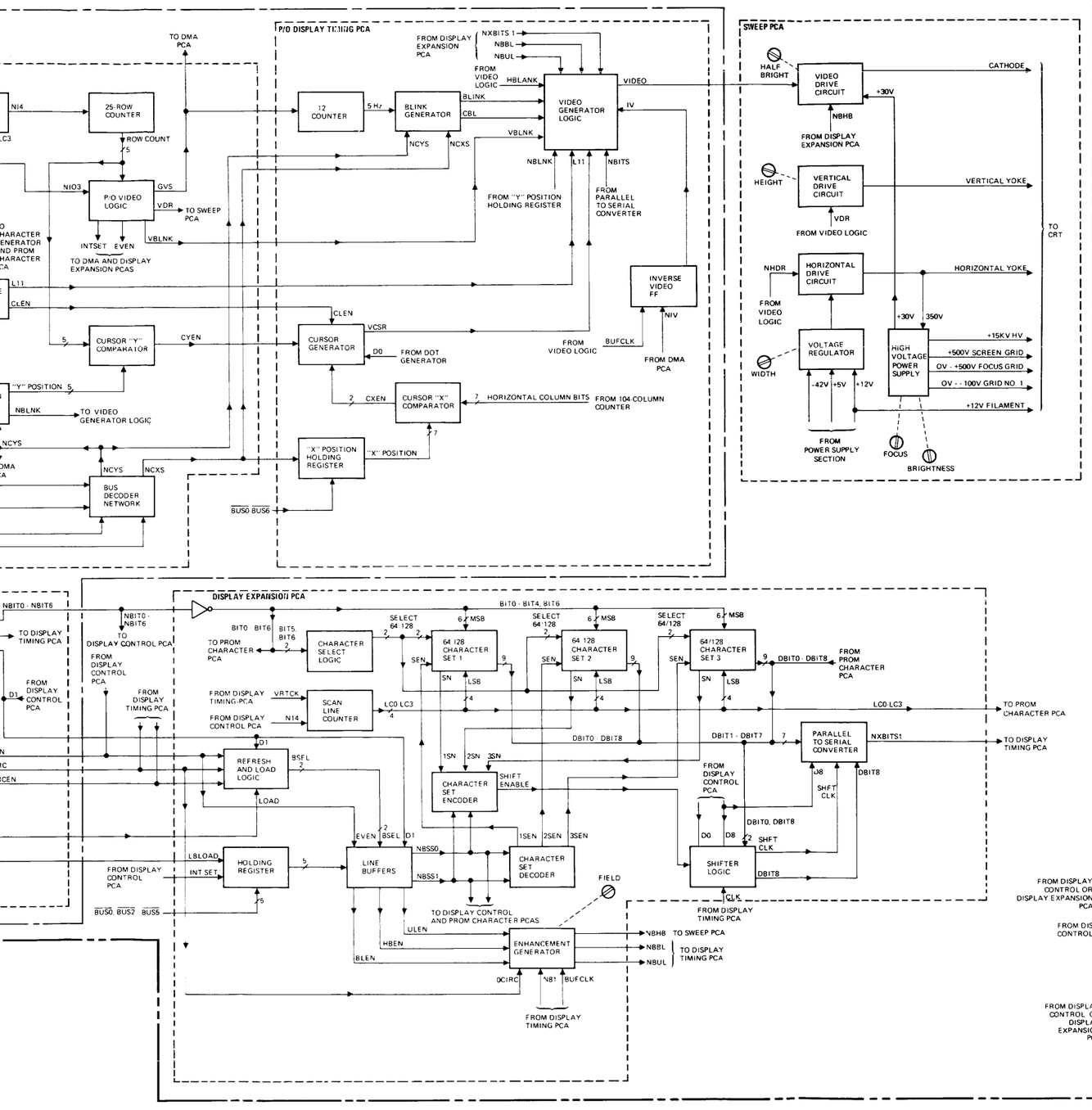


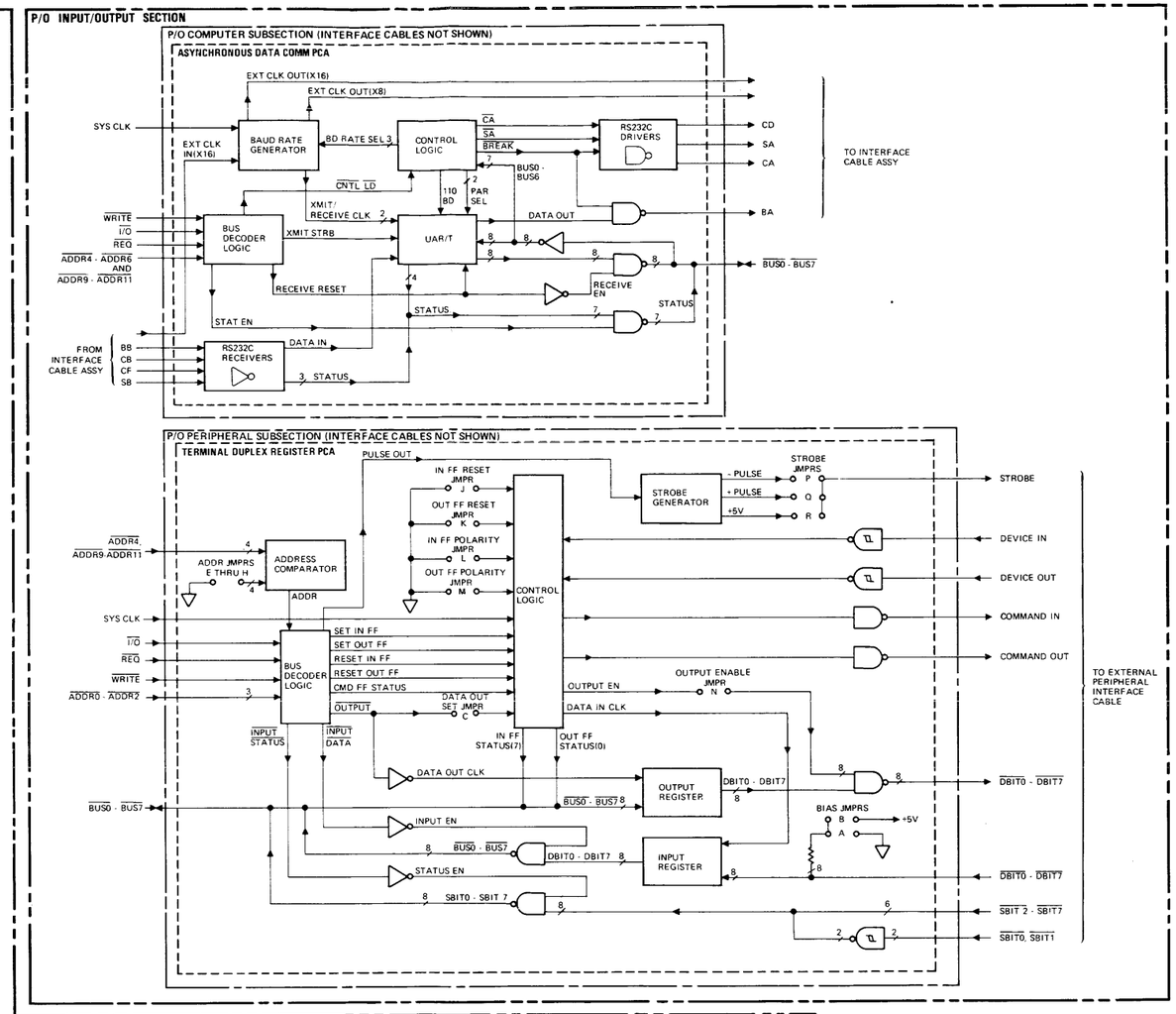
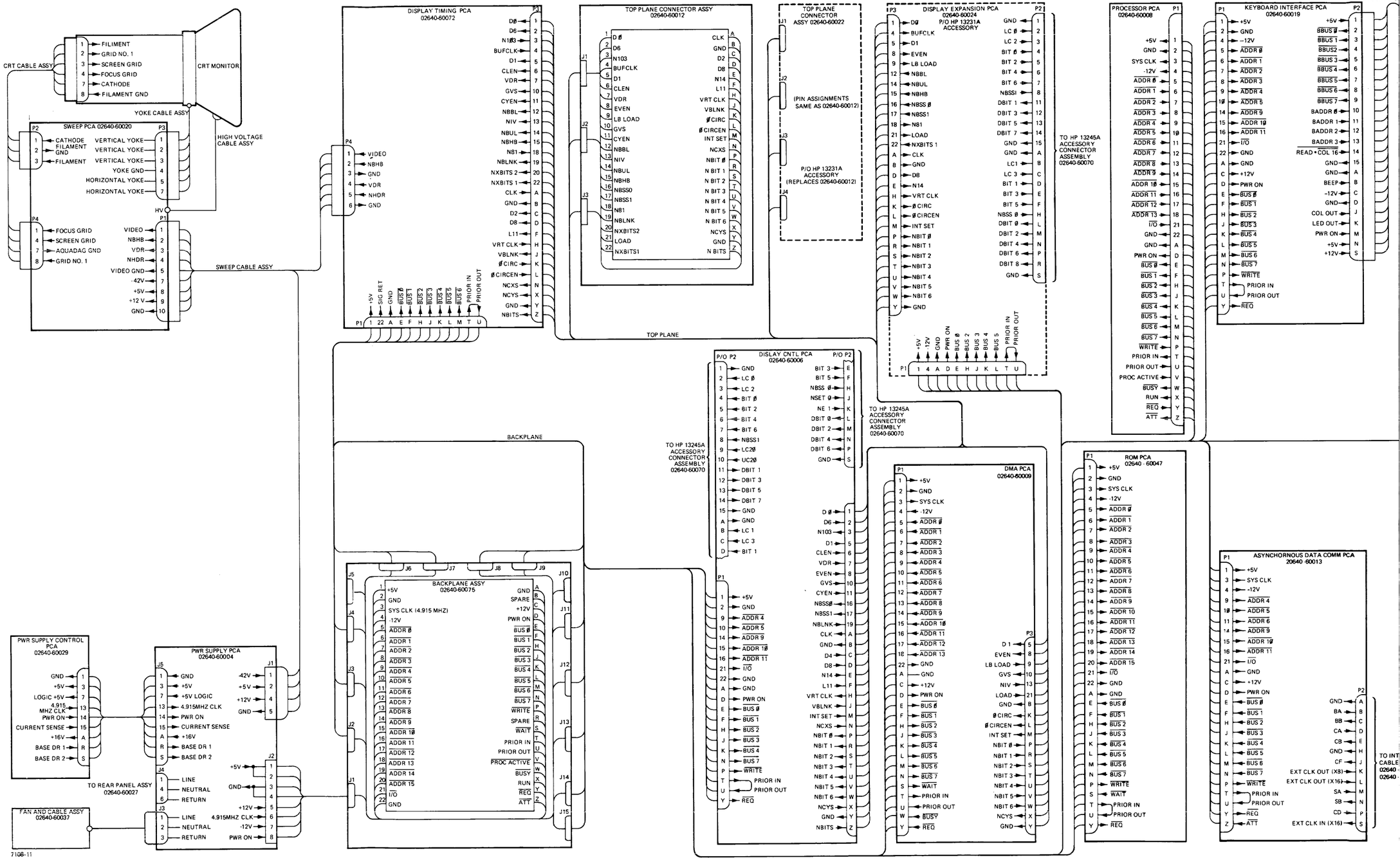


Figure 2-2. Detailed Block Diagram (Sheet 2 of 2)


CRT CABLE ASSY
FILIMENT
GRID NO. 1
SCREEN GRID
FOCUS GRID
CATHODE
FILAMENT GND
CRT MONITOR
YOKE CABLE ASSY
HIGH VOLTAGE CABLE ASSY
SWEEP PCA 02640-60020
CATHODE
FILAMENT
GND
FILAMENT
VERTICAL YOKE
VERTICAL YOKE
VERTICAL YOKE
YOKE GND
HORIZONTAL YOKE
HORIZONTAL YOKE
HV
FOCUS GRID
SCREEN GRID
AQUADAG GND
GRID NO. 1
VIDEO
NBHB
VDR
NHDR
VIDEO GND
-42V
+5V
+12 V
GND
SWEEP CABLE ASSY
DISPLAY TIMING PCA 02640-60072
VIDEO
NBHB
GND
VDR
NHDR
GND
+5V
SIG RET
GND
BUS Ø
BUS 1
BUS 2
BUS 3
BUS 4
BUS 5
BUS 6
PRIOR IN
PRIOR OUT
D Ø
D6
N103
BUFCLK
D1
CLEN
VDR
GVS
CYEN
NBBL
NIV
NBUL
NBHB
N81
NBLNK
NXBITS 2
NXBITS 1
CLK
GND
D2
D8
L11
VRT CLK
VBLNK
Ø CIRC
Ø CIRCEN
NCXS
NCYS
GND
NBITS
TOP PLANE CONNECTOR ASSY 02640-60012
TOP PLANE CONNECTOR ASSY 02640-60022
(PIN ASSIGNMENTS SAME AS 02640-60012)
P/O HP 13231A ACCESSORY (REPLACES 02640-60012)
TOP PLANE
DISPLAY EXPANSION PCA 02640-60024 P/O HP 13231A ACCESSORY
TO HP 13245A ACCESSORY CONNECTOR ASSEMBLY 02640-60070
PROCESSOR PCA 02640-60008
KEYBOARD INTERFACE PCA 02640-60019
KEYBOARD CA
DISLAY CNTL PCA 02640-60006
TO HP 13245A ACCESSORY CONNECTOR ASSEMBLY 02640-60070
BACKPLANE
BACKPLANE ASSY 02640-60075
DMA PCA 02640-60009
ROM PCA 02640 - 60047
ASYNCHORNOUS DATA COMM PCA 20640 -60013
TO INT CABLE 02640 02640-
PWR SUPPLY CONTROL PCA 02640-60029
PWR SUPPLY PCA 02640-60004
GND
+5V
LOGIC +5V
4.915 MHZ CLK
PWR ON
CURRENT SENSE
+16V
BASE DR 1
BASE DR 2
-42V
+5V
+12V
GND
+5V LOGIC
4.915MHZ CLK
PWR ON
CURRENT SENSE
+16V
BASE DR 1
BASE DR 2
LINE
NEUTRAL
RETURN
TO REAR PANEL ASSY 02640-60027
FAN AND CABLE ASSY 02640-60037
4.915MHZ CLK
-12V
PWR ON
7108-11

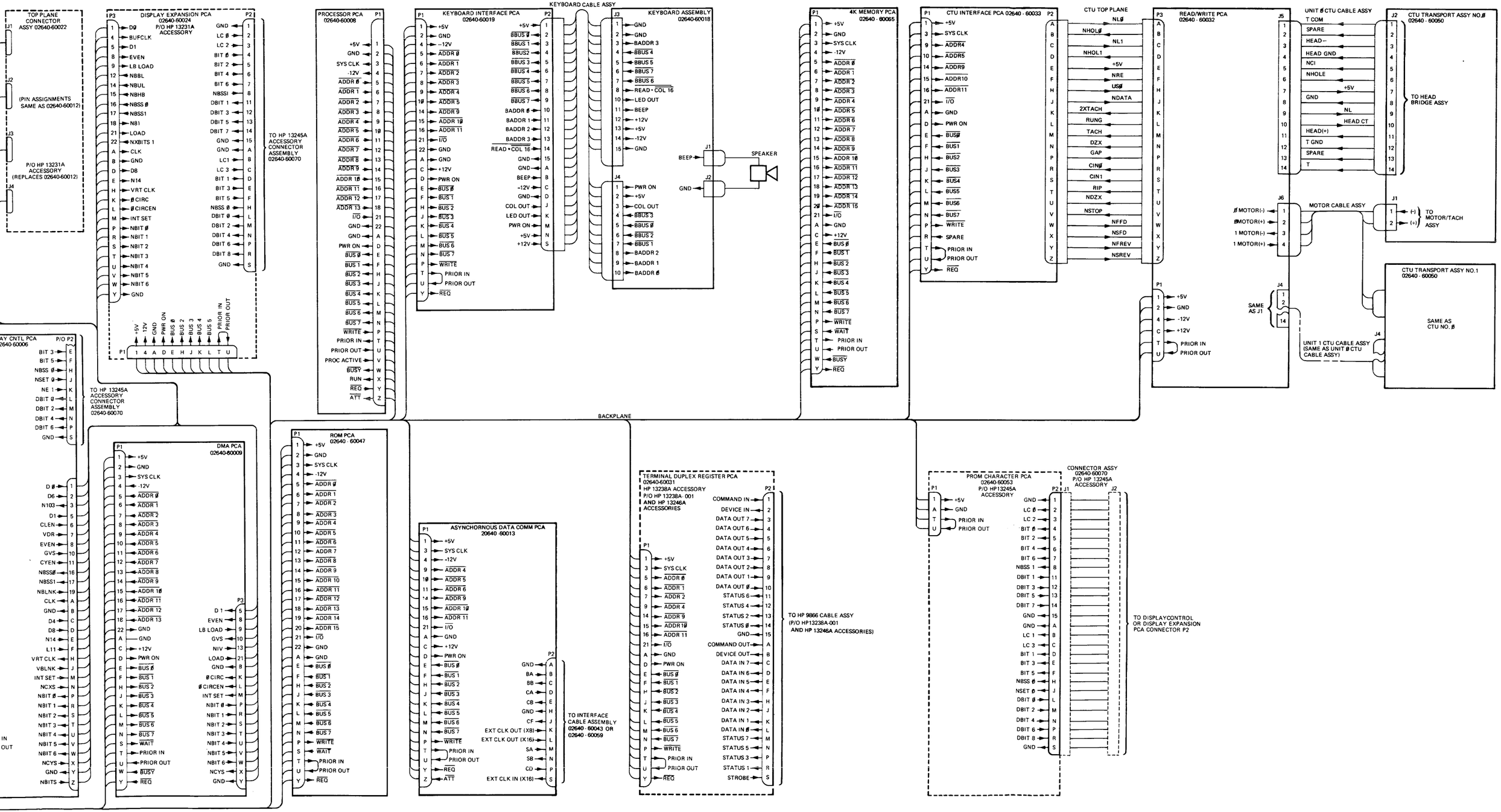


Figure 2-3. Terminal Interconnecting Cable Diagram

SERVICE

SECTION III

3-1. INTRODUCTION

This section contains troubleshooting information for isolating mini data station (terminal) malfunctions to a replaceable assembly, alignment and adjustment procedures, preventive maintenance procedures, and instructions for using special test equipment.

WARNING

Hazardous voltages are present inside equipment. The procedures contained in this section shall be performed only by qualified service personnel.

VORSICHT

Innerhalb des Geräts bestehen gefährliche Spannungen. Die in diesem Abschnitt enthaltenen Arbeiten dürfen nur durch Betriebsfachpersonal durchgeführt werden.

ATTENTION

Des tensions dangereuses sont présentes à l'intérieur du matériel. Les opérations décrites dans cette section ne devront être effectuées que par un personnel qualifié.

AVVISO

Pericolo: Alta tensione presente in questa apparecchiatura. Le procedure contenute in questa sezione debbono essere effettuate soltanto da qualificato personale di servizio.

ADVERTENCIA

Hay voltaje peligroso en el interior de este equipo. Los procedimientos expuestos en esta sección sólo deberá llevarlos a cabo el personal de servicio calificado.

高圧危険

内部装置に危険な高電圧がきています。この章にある処置や手続に関しては、専門のサービスマンによってのみ行なって下さい。

3-2. TROUBLESHOOTING

3-3. GENERAL TROUBLE ISOLATION PROCEDURES

The majority of apparent terminal malfunctions are caused by incorrect operation. Therefore, before attempting any detailed trouble isolation procedures, verify that a terminal malfunction truly exists as follows:

a. Ensure that terminal is properly installed (power cord connected and fuse properly installed) and is set to correct operating mode.

b. Ensure that special function keys are being used correctly and in correct sequence.

c. Determine whether or not any recent service routines (accessory installation, cables removed or installed, adjustments performed, etc.) have been performed on terminal. If so, check workmanship.

d. Check all connections in accordance with paragraph 3-4.

e. Check keyboard and communication group in accordance with paragraph 3-5.

f. Perform terminal self test in accordance with paragraph 3-6.

g. Check storage subsection in accordance with paragraph 3-7.

3-4. CONNECTION INSPECTION

Set mainframe rear panel AC POWER switch to OFF, disconnect power cord, and inspect cable connections as follows:

a. Ensure that Keyboard Cable Assembly hood connector is firmly connected to Keyboard Interface PCA.

b. Ensure that interface cable assembly hood connector is firmly connected to Asynchronous Data Comm PCA.

c. If installed, ensure that peripheral interface cable assembly hood connector is firmly connected to Terminal Duplex Register PCA.

d. Open terminal mainframe to its full open position in accordance with paragraph 1-2 and check that all PCA's are firmly seated in Backplane Connector Assembly.

e. Ensure that Power Supply Control PCA is firmly seated in Power Supply PCA connector J5.

f. Ensure that all internal cable assembly connectors are correctly and firmly connected.

3-5. KEYBOARD AND COMMUNICATION GROUP CHECKOUT

The major part of the terminal keyboard can be quickly checked for proper operation by setting the terminal for local operation (REMOTE key up), pressing each of the keys listed in table 3-1, and obtaining the listed results. If an incorrect result is observed, a malfunction exists in either the Keyboard Interface PCA or Keyboard PCA. (Removal and replacement procedures are contained in section IV.) The communication group including the Asynchronous Data Comm PCA can be quickly checked for proper operation as follows:

a. Replace existing cable assembly hood connector connected to Asynchronous Data Comm PCA with HP Test Hood, part no. 02640-60077. Keyboard TRANSMIT indicator will light.

b. Depress REMOTE key, set BAUD RATE switch to 110, and DUPLEX switch to FULL.

c. Hold down any character key and check that associated character is repeatedly displayed across display monitor at a slow rate of speed for as long as the key is held down.

Note: Delete symbol (white square) may appear on display monitor when switching baud rates.

d. While holding down character key, increase baud rate to 150 and then to 300 and check that displayed character repetition rate increases as baud rate increases. If operation is not as stated, a malfunction probably exists in Asynchronous Data Comm PCA or Keyboard Assembly. (Baud rates above 300 will not increase character repetition rate.)

e. Set DUPLEX switch to HALF.

f. Depress any character key once and check that associated character is displayed twice on display monitor. If operation is not as stated, a malfunction probably exists in Asynchronous Data Comm PCA or Keyboard Assembly.

Table 3-1. Keyboard Checkout Keys

KEY	RESULTS
DISPLAY FUNCTIONS	DISPLAY FUNCTIONS indicator lights
1	1 is displayed
Q or Q	Q or q is displayed
Z or z	Z or z is displayed
L	L is displayed
Numeric Pad 1	1 is displayed
Numeric Pad 4	4 is displayed
CNTL G	🔔 is displayed (Option 001 terminals only)
Release DISPLAY FUNCTIONS key and again press CNTL G keys.	Audible "beep" is generated

3-6. SELF TEST

The self-test feature provides an overall check of the terminal making it possible to quickly analyze and isolate most terminal malfunctions. This test does not check the storage subsection modules. Refer to paragraph 3-7 for storage subsection test. (Removal and replacement procedures are contained in Section IV.) Perform the test as follows:

a. Set mainframe rear panel AC POWER switch to on and observe keyboard. Some keyboard indicators may flash on and then off. If any indicators with the exception of TRANSMIT indicator remain lighted, a malfunction exists in Processor PCA.

b. Check that blinking cursor appears in upper left corner of display monitor approximately seven seconds after terminal is energized. This verifies that Sweep, Processor, ROM, Display Memory Access (DMA), Display Control, and Display Timing PCA's are operating correctly. If cursor does not appear, malfunction probably exists in Sweep PCA.

c. Press Keyboard TEST key and observe following sequence of events:

(1) Keyboard indicators light. If no indicators light, malfunction probably exists in Power Supply or Power Supply Control PCA.

(2) ROM PCA ROM's are checked. In most cases, if a ROM malfunction is encountered, monitor will display "ROM TEST FAILED", indicating a defective ROM PCA.

(3) Entire display including cursor momentarily blanks which checks display portions of Processor, DMA, Display Control, and Display Timing PCA's. If display does not clear (blank), malfunction probably exists in Display Control PCA.

(4) While display is still blanked, the 4K Memory PCA RAM's are checked. In most cases, if a RAM malfunction is encountered, monitor will display "RAM TEST FAILED" indicating a defective 4K Memory PCA.

(5) An audible "beep" is generated. If not, keyboard speaker may be defective or a malfunction probably exists in Processor PCA.

(6) Entire character set is displayed and, after printout, blinking cursor appears in first column of next lower line. The test pattern contains all available symbols and display enhancements. Last line of test pattern displays status of terminal. Refer to *HP 2644A Mini Data Station Owner's Manual* for status byte definitions and correct test pattern displays. If test pattern is incorrect, refer to paragraph 3-8.

3-7. STORAGE SUBSECTION CHECKOUT

The storage subsection checkout provides a check of the entire terminal, including the storage subsection, making it possible to quickly verify proper terminal operation and, when a malfunction exists, to isolate most malfunctions to a replaceable module. (Removal and replacement procedures are contained in Section IV.) Perform the checkout in accordance with steps a through m. If a malfunction occurs, note the checkout step letter and refer to table 3-2. Table 3-2 is keyed to the checkout by step letter and contains a list of malfunctions that could occur for each step (SYMPTOM) and associated lists of PROBABLE CAUSE and CORRECTIVE ACTION procedures. If more than one probable cause is listed for a specific symptom, check the probable causes in the order listed. If more than one corrective action is listed for a specific probable cause, perform the corrective actions in the order listed. After any corrective action has been performed,*check if the malfunction has been corrected.* If the malfunction persists, check the next probable cause, perform the corrective action(s), and again check if the malfunction has been corrected. After any malfunction has been corrected, repeat this entire checkout procedure to ensure proper terminal operation.

a. Open terminal to its half open position in accordance with paragraph 1-2.

b. Using at least two tape cartridges, check that cartridges can be easily inserted and ejected for both UNIT 0 and UNIT 1.

c. Perform terminal self test in accordance with paragraph 3-6.

d. Press RESET TERMINAL key and check that display clears and blinking cursor appears in upper-left corner of display.

CAUTION

Do not use tape cartridges containing data you wish to save when performing the following checkout procedures. Data previously stored on tape will be overwritten with test data.

Note: Many of the following test sequences can be individually duplicated using the HP CTU Tester discussed in paragraph 3-19. Whenever it is desired to perform such a test sequence more than once, it is recommended that the CTU Tester be used rather than to repeat the entire checkout procedure.

e. Set cartridge protect tab on both tape cartridges to RECORD position, insert tape cartridges in UNIT 0 and UNIT 1, and observe the following sequence of events.

(1) SEARCHING message replaces cursor in upper-left corner of display and, simultaneously, the tape cartridges sequentially rewind to beginning-of-tape (BOT) and then search forward to load point (LP). (Tape motion; fast reverse then slow forward.)

(2) When both tapes are at LP, cursor replaces SEARCHING message on display and both eject buttons light.

f. Press GREEN key and then TEST key and observe the following sequence of events.

Note: If a malfunction occurs while testing either CTU Transport Assembly, test will halt and the eject button on the CTU Transport Assembly under test when the malfunction occurred will be lighted.

(1) UNIT 0 eject button light starts blinking indicating start of a complete test for UNIT 0. Test sequence is as follows:

(a) Worst case test pattern (one record of 128 "%Z" characters) is recorded on tape. (Tape motion; slow forward.)

(b) Tape is backspaced over recorded test pattern. (Tape motion; slow reverse.)

(c) Recorded test pattern is read and verified and an end-of-file mark recorded. (Tape motion; slow forward.)

(2) UNIT 0 eject button light stops blinking and remains on indicating successful completion of UNIT 0 test.

(3) Two self-test patterns momentarily appear on display indicating the successful completion of two basic terminal self-test sequences.

(4) UNIT 1 eject button starts blinking indicating start of complete test for UNIT 1. Sequence of events for UNIT 1 test is identical to sequence of events for UNIT 0 test described in substeps (1)(a) through (1)(c) above.

(5) Another self-test pattern appears and remains on display and both eject buttons remain lighted indicating the successful completion of UNIT 1 test.

g. Press GREEN, REWIND, and L. TAPE keys and check that UNIT 0 tape cartridge rewinds to BOT (tape motion; fast reverse) and, after tape stops at BOT, check that UNIT 0 eject button is no longer lighted.

h. Press GREEN, REWIND, and R. TAPE keys and check that UNIT 1 performs the same as UNIT 0 in step g above.

i. Swap tape cartridges between UNIT 0 and UNIT 1.

j. Press RESET TERMINAL and, after cartridges have rewound and both eject button lights are on, press READ key. Check that a line of "%Z" characters are read from UNIT 0 and appear on display. (Tape motion; slow forward.)

k. Press GOLD, FROM: R. TAPE, and READ keys and check that a line of "%Z" characters are read from UNIT 1 and appear on display. (Tape motion; slow forward.)

l. Rewind both tape cartridges (steps g and h above) and remove cartridges from terminal.

m. Firmly grasp mainframe top cover in one hand and release safety latch by pressing it inboard with other hand. Then, using both hands, carefully lower top cover to its closed position.

Table 3-2. Storage Subsection Troubleshooting Guide

STEP	SYMPTOM	PROBABLE CAUSE	CORRECTIVE ACTION
	Note: Some of the listed PROBABLE CAUSE malfunctions are preceded by an asterisk (*). The asterisk denotes that the malfunction can be further checked or verified by using the HP CTU Tester as discussed in paragraph 3-19. Whenever such a malfunction is encountered, it is recommended that the tester be used to verify the malfunction before performing any CORRECTIVE ACTION instructions.		
a	Not applicable.		
b	Tape cartridge does not insert easily or does not seat properly.	1. Defective tape cartridge. 2. CTU Transport Assy and mainframe front bezel not properly aligned. 3. Defective CTU Base Assy.	Replace tape cartridge. Align transport and bezel (paragraph 1-9). Replace CTU Transport Assy.
	Tape cartridge does not fully eject.	Same as causes 1 through 3 above.	Same as above.
	Tape cartridge ejects from terminal.	Defective CTU Base Assy.	Replace CTU Transport Assy.
c	Not applicable.		

Table 3-2. Storage Subsection Troubleshooting Guide (Cont)

STEP	SYMPTOM	PROBABLE CAUSE	CORRECTIVE ACTION
d	Display does not clear and/or cursor does not appear.	1. Operator error. 2. Basic terminal malfunction.	Press RESET TERMINAL key. Perform terminal self test (paragraph 3-6).
e(1)	SEARCHING message does not appear and neither tape cartridge rewinds.	1. CTU Top Plane not properly connected. 2. CTU Interface and/or Read/Write PCA not properly connected. *3. Defective top plane or PCA top connectors. *4. Defective bus decoder and timing logic, command logic, or tape motion decoder. *5. Defective amplifier select logic or CTU drive circuits.	Reinstall top plane on CTU Interface and Read/Write PCA top connectors. Reinstall PCA's in Backplane Assy. Use CTU Tester in its ON LINE mode. Verify malfunction and, if necessary, replace top plane and/or PCA's. Replace CTU Interface PCA. Replace Read/Write PCA.
	NO TAPE message appears on display and only one tape cartridge rewinds.	1. Tape cartridge not seated properly in CTU Transport Assy with lighted eject button. 2. Defective tape cartridge. *3. Defective Head Bridge Assy in CTU Transport Assy with lighted eject button. *4. Defective cartridge detect circuit, amplifier select circuit, or CTU drive circuits. *5. Defective command logic, hole detect logic, or status bus drivers.	Eject and reinsert tape cartridge in transport assy. Replace tape cartridge. Replace CTU Transport Assy. Replace Read/Write PCA. Replace CTU Interface PCA.
	NO TAPE message appears on display and neither tape cartridge rewinds.	*1. Defective bus decoder and timing logic, command logic, hole detect logic, or tape motion decoder. *2. Defective amplifier select logic or CTU drive circuits.	Replace CTU Interface PCA. Replace Read/Write PCA.

Table 3-2. Storage Subsection Troubleshooting Guide (Cont)

STEP	SYMPTOM	PROBABLE CAUSE	CORRECTIVE ACTION
e(1) cont	RUNOFF message appears on display.	1. Defective tape cartridge in CTU Transport Assy with lighted eject button.	If tape has run off either tape hub, either rethread (paragraph 4-11) or replace tape cartridge. If tape is attached to both hubs, rewind approximately 1/2 inch of tape by manually rotating cartridge belt drive puck.
		*2. Defective Head Bridge Assy in CTU Transport Assy with lighted eject button.	Replace CTU Transport Assy.
		*3. Defective hole detect logic or hole detect flip-flop.	Replace CTU Interface PCA.
	Both tape cartridges rewind, but neither searches forward to LP.	*1. Defective command logic or tape motion decoder.	Replace CTU Interface PCA.
		*2. Defective CTU drive circuits or feedback circuits.	Replace Read/Write PCA.
	One tape cartridge rewinds and stops at LP, but no tape motion on other tape cartridge.	*1. Defective Motor/ Tachometer Assy on CTU Transport Assy with lighted eject button.	Replace CTU Transport Assy.
e(1) cont		*2. Defective amplifier select logic or CTU drive circuits.	Replace Read/Write PCA.
		*3. Defective Head Bridge Assy on CTU Transport Assy with lighted eject button.	Replace CTU Transport Assy.
e(2)	SEARCHING message remains on display and neither eject button is lighted.	*Defective bus decoder and timing logic or command logic.	Replace CTU Interface PCA.
	Cursor appears on display, but neither eject button is lighted.	*Defective command logic.	Replace CTU Interface PCA.
	Cursor appears on display, but only one eject button is lighted.	1. Defective indicator lamp DS1 on unlighted eject button.	Replace DS1.
		2. Defective Head Bridge Assy on unlighted CTU Transport Assy.	Replace CTU Transport Assy.

Table 3-2. Storage Subsection Troubleshooting Guide (Cont)

STEP	SYMPTOM	PROBABLE CAUSE	CORRECTIVE ACTION
e(2) cont		*3. Defective command logic.	Replace CTU Interface PCA.
f(1)	PROTECTED TAPE message appears on display.	1. Operator error.	Eject tape cartridge, set cartridge protect tab to RECORD position, and reinsert tape cartridge in UNIT 0.
		*2. Defective Head Bridge Assy.	Replace UNIT 0 CTU Transport Assy.
		*3. Defective unit/function decoder or write current circuit.	Replace Read/Write PCA.
		*4. Defective command logic.	Replace CTU Interface PCA.
	RUNOFF message appears on display.	Same as STEP e(1) RUNOFF message SYMPTOM.	
	READ FAIL message appears on display. (Also see END OF DATA message in paragraph 3-24.)	1. Defective tape cartridge.	Condition UNIT 0 tape (paragraph 3-18) or, if malfunction persists, replace tape cartridge.
		*2. Defective magnetic head.	Clean and degauss UNIT 0 magnetic head (paragraph 3-16 and 3-17) or, if malfunction persists, replace UNIT 0 CTU Transport Assy.
		*3. Defective data I/O buffer, shift register, or encoder/decoder logic.	Replace CTU Interface PCA.
		*4. Defective unit/function decoder, write current circuit, read select switch, read amplifier circuit, or gap detect circuit.	Replace Read/Write PCA.
		*5. Defective Motor/ Tachometer Assy.	Replace UNIT 0 CTU Transport Assy.
F(2)	Not applicable.		
f(3)	ROM or RAM TEST FAIL messages appear on display, test patterns do not appear, or incorrect test patterns appear.	Basic terminal malfunction.	Perform terminal self test (paragraph 3-6).

Table 3-2. Storage Subsection Troubleshooting Guide (Cont)

STEP	SYMPTOM	PROBABLE CAUSE	CORRECTIVE ACTION
f(4) and f(5)	Same as f(1) except use UNIT 1 in lieu of UNIT 0.		
g	Tape cartridge does not rewind.	1. Operator error.	Repeat key stroke sequence.
		*2. Defective command logic or tape motion decoder.	Replace CTU Interface PCA.
h	Same as step g.		
i	Not applicable.		
j	No characters appear on display.	1. Operator error.	Repeat key stroke sequence.
		*2. Defective bus decoder and timing logic, command logic, data I/O logic, shift register, or encoder/decoder logic.	Replace CTU Interface PCA.
	Blanks appear between displayed characters.	1. Defective tape cartridges.	Condition tapes or replace tape cartridges (paragraph 3-18).
		*2. CTU Transport speeds not balanced.	Perform speed adjustment (paragraph 3-14).
	READ FAIL message appears on display.	*1. CTU Transport speeds not balanced.	Perform speed adjustment (paragraph 3-14).
		*2. Defective magnetic head.	Clean and degauss UNIT 0 magnetic head (paragraph 3-16 and 3-17) or, if malfunction persists, replace UNIT 0 CTU Transport Assy.
k	Same as step j except use UNIT 1 in lieu of UNIT 0.		
l and m	Not applicable.		

3-8. DETAILED TROUBLE ISOLATION PROCEDURES

Any terminal malfunctions not isolated and corrected by the procedures contained in paragraphs 3-3 through 3-7 can be isolated to a replaceable assembly by performing in sequence the procedures presented in figure 3-1. Some corrective action procedures in figure 3-1 consist of more than one replacement instruction. When these are encountered, replace the first assembly listed and *check if the malfunction has been corrected.* (Removal and replacement procedures are contained in Section IV.) If the malfunction persists, reinstall the first assembly listed, replace the second assembly listed, and again check if the malfunction has been corrected. As an additional troubleshooting aid, figure 2-3 provides a terminal interconnecting cabling diagram illustrating source and destination signal flow between replaceable assemblies. After any malfunction has been corrected, use the terminal's self-test feature to ensure proper operation.

3-9. ALIGNMENT AND ADJUSTMENT

All alignment and adjustment procedures for the terminal and its add-on accessories are contained in the following paragraphs. Unless otherwise specified, these procedures can be performed individually or in any desired sequence.

Note: After performing any alignment or adjustment procedures, always use the terminals self-test feature (paragraph 3-6) to ensure proper terminal operation.

3-10. POWER SUPPLY VOLTAGE ADJUSTMENT

a. Open terminal mainframe to its half open position in accordance with paragraph 1-2.

b. Remove power supply housing (bottom left side of mainframe) by unlatching two snap locks on front of housing and pulling housing up and out toward front of mainframe.

c. Connect multimeter between +5V diode CR17 (see figure 3-2) and chassis ground.

d. Connect power cord between power source and mainframe rear panel LINE connector.

e. Set rear panel AC POWER switch to on position and ensure that neither CTU motor is running.

f. Check for multimeter indication between +4.85V and +5.25V at diode CR17.

g. Using multimeter, check for +11.4V to +12.6V at diode CR13 and for - 11.4V to - 12.6V at diode CR14 (see figure 3-2). If necessary, adjust +5V potentiometer R14 until 12V voltage levels are as specified. If adjustment is required, proceed to step h. If adjustment is not required, skip to step i.

h. Using multimeter, check that +5V voltage level is still within tolerances specified in step f.

i. Using tape conditioning procedures in paragraph 3-18 and multimeter, check for +11.4V to +12.6V at diode CR13 while tape is winding forward and for -11.4V to -12.6V at diode CR14 while tape is rewinding. If necessary, readjust +5V potentiometer R14 until 12V voltage levels are as specified. If readjustment is required, repeat steps g through i. If readjustment is not required, proceed to step j.

j. Set rear panel AC POWER switch to OFF and disconnect multimeter from power supply.

k. Replace power supply housing and secure in place with two snap locks.

l. Close terminal mainframe.

3-11. BRIGHTNESS, HALF BRIGHT, AND FOCUS ADJUSTMENTS

Due to product design, these adjustments seldom need be performed. However, minor adjustment can be made to each potentiometer (see figure 3-3) to suit individual preferences by opening the terminal mainframe to its half open position in accordance with paragraph 1-2, energizing the terminal, and adjusting the applicable potentiometer for the desired display appearance. If extensive repair or replacement procedures have been performed on the terminal, it is suggested that the adjustment procedure below be performed in its entirety to ensure optimum terminal performance.

This procedure requires the use of the HP Display Test Module, part no. 02640-60063. The brightness, half bright, and focus adjustments are interactive and, therefore, must be performed together. Perform the adjustments as follows:

a. Open terminal mainframe to its half open position in accordance with paragraph 1-2.

b. Insert connector removal tool under Top Plane Connector Assembly as shown in figure 1-5 and remove assembly by pressing down on removal tool handle.

c. Remove Display Memory Access (DMA) PCA from Backplane Assembly.

d. If necessary, rearrange backplane PCA configuration to that shown in figure 1-1.

e. Install Display Test Module on top connectors of Display Timing and Display Control PCA'S so that test module cable is toward front of mainframe.

f. Connect test module cable plug to Display Timing PCA +5V red test jack located on top front of PCA.

g. Connect power cord between ac power source and mainframe rear panel LINE connector.

h. Set rear panel AC POWER switch to on position.

i. Set test module HALF BRIGHT switch to off position, INVERSE VIDEO switch to off position, and DOTS/CROSSHATCH switch to DOTS.

j. Adjust BRIGHTNESS R37 (see figure 3-3) for desired display brightness.

k. Set test module HALF BRIGHT switch to on position, remove button covering CRT shield HALF BRIGHT adjustment access hole, and adjust HALF BRIGHT R5 for desired display half brightness.

l. Repeat steps i, j, and k until desired display contrast is obtained between full bright and half bright.

m. Set test module HALF BRIGHT switch to off position.

n. Adjust FOCUS R33 (see figure 3-3) for best overall display sharpness.

o. If desired focus cannot be obtained, adjust display brightness slightly lower and repeat steps i through n.

p. Set rear panel AC POWER switch to OFF and reinstall button to cover HALF BRIGHT adjustment access hole.

q. Secure CRT shield in place by pressing four nylon snap fasteners into mounting holes.

r. Disconnect test module cable plug from Display Timing PCA and disconnect test module from Display Timing and Display Control PCA's.

s. Reinstall DMA PCA into vacated Backplane Assembly connector and reinstall Top Plane Connector Assembly on DMA, Display Timing, and Display Control PCA's.

3-12. DISPLAY EXPANSION FIELD ADJUSTMENT

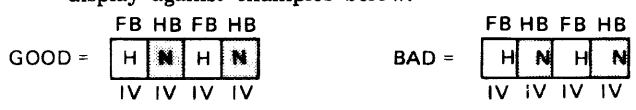
After initial installation of the HP 13231A Display Enhancements Accessory, check and, if necessary, adjust the Display Expansion PCA as follows:

a. Open terminal mainframe to its half open position in accordance with paragraph 1-2.

b. Connect power cord between ac power source and mainframe rear panel LINE connector.

c. Set rear panel AC POWER switch to on position.

d. Using keyboard, set terminal for local operation (REMOTE key up) and press each of the following keys once: CAPS LOCK, CNTL, f_1, B, H, CNTL, f_1 J, N, CNTL, f_1, B, H, CNTL, f_1, J, N. Compare display against examples below.



WHERE: FB = full bright enhancement
HB = half bright enhancement
IV = inverse video enhancement

e. If necessary, adjust Display Expansion PCA FIELD potentiometer R10 to center full bright and half bright enhancements over characters displayed on monitor.

f. Set rear panel AC POWER switch to OFF and close terminal mainframe.

3-13. DISPLAY RASTER ALIGNMENT AND ADJUSTMENT

This procedure requires the use of the HP Display Test Module, part no. 02640-60063. Align and adjust the display raster as follows:

a. Open terminal mainframe to its half open position in accordance with paragraph 1-2 and remove CRT shield as follows:

(1) Insert connector removal tool handle between front edge of CRT shield and front edge of mainframe top cover so that connector removal tool handle is between CRT shield and mounting bracket. (See figure 1-2 for mounting bracket location.)

(2) Using connector removal tool as a lever (push up on bottom of tool), force front of CRT shield downward until front two shield fasteners are free of mounting holes. (see figure 1-2.)

(3) Remove remaining fasteners securing CRT shield in place by pulling down on shield until all fasteners are free of mounting holes. Do not attempt to remove fasteners from CRT shield.

b. Insert connector removal tool under Top Plane Connector Assembly as shown in figure 1-5 and remove assembly by pressing down on removal tool handle.

c. Remove DMA PCA from Backplane Assembly.

d. If necessary, rearrange backplane PCA configuration to that shown in figure 1-1.

e. Install Display Test Module on top connectors of Display Timing and Display Control PCA's so that test module cable is toward front of mainframe.

f. Connect test module cable plug to Display Timing PCA red test jack located on top front of PCA.

g. Connect power cord between ac power source and mainframe rear panel LINE connector.

h. Set rear panel AC POWER switch to on position.

i. Set test module HALF BRIGHT switch to off position, INVERSE VIDEO switch to on position, and DOTS/CROSSHATCH switch to center off position.

j. The monitor should display an inverse video rectangular pattern. If no pattern is displayed, adjust

BRIGHTNESS R37 (see figure 3-3) until pattern is displayed. If this step is required, perform brightness and focus adjustments in accordance with paragraph 3-11 after completing raster alignment and adjustment procedures.

WARNING

High voltage is present on exposed portions of Yoke Cable Assembly.

VORSICHT

An den offenen Stellen des Joch-Kabelsatzes (Yoke Cable Assembly) besteht Hochspannung!

ATTENTION

Du courant haute tension passe dans les parties exposées de l'ensemble de câbles de culasse (Yoke Cable Assembly).

AVVISO

Voltaggio ad alta tensione presente su parti scoperte della linea montaggio di cavo collegamento (Yoke Cable Assembly).

ADVERTENCIA

Hay voltaje peligroso en las partes al descubierto del conjunto de cable de horquilla (Yoke Cable Assembly).

高圧危険

ヨーク・ケーブルアセンブリの露出部には、高電圧がかかってます。

k. Loosen yoke retainer screw and rotate yoke (see figure 3-3) until displayed rectangle is horizontal and parallel to monitor frame.

CAUTION

Do not tighten yoke retainer screw any more than necessary to keep yoke from sliding on the neck of the CRT (finger tight). Overtightening can damage CRT.

l. Secure yoke in place by tightening yoke retainer screw.

m. Rotate centering magnets (black tabs) until displayed rectangle is centered on monitor screen.

n. Adjust WIDTH R28 until displayed rectangle is 9.50 in. (24.13 cm) wide.

o. Adjust HEIGHT R10 until displayed rectangle is 4.75 in (12.065 cm) high.

p. Set rear panel AC POWER switch to OFF and secure CRT shield in place with fasteners.

q. Disconnect test module cable plug from Display Timing PCA and disconnect test module from Display Timing and Display Control PCA's.

r. Reinstall DMA PCA into vacated Backplane Assembly connector and reinstall Top Plane Connector Assembly on DMA, Display Timing, and Display Control PCA's.

s. Close terminal mainframe and check for correct raster alignment.

3-14. CTU TRANSPORT ASSEMBLY SPEED ADJUSTMENT

This adjustment procedure requires the use of the HP CTU Tester, part no. 02640-60082 and the HP Checkout Cartridge, part no. 02640-60096. Perform the adjustment as follows:

a. Open terminal mainframe to its half open position in accordance with paragraph 1-2.

b. Insert connector removal tool under CTU Top Plane Assembly and remove assembly by pressing down on the removal tool handle. Use of the removal tool is illustrated in figure 1-5.

c. Install CTU Tester on top connectors of CTU Interface and Read/Write PCA's so that tester indicator lamps are closest to rear of terminal mainframe.

d. Set CTU Tester's UNIT switch to 0, ON LINE/OFF LINE switch to OFF, RVS/FWD switch to FWD, and IPS switch to 10.

e. Remove any tape cartridges inserted in terminal.

f. Connect power cord between ac power source and mainframe rear panel LINE connector.

g. Set rear panel AC POWER switch to on position.

h. Insert Checkout Cartridge in UNIT 0 CTU Transport Assembly.

Note: Maximum brilliance of tester 10 IPS ADJ indicator lamp indicates that CTU Transport Assembly motor is rotating at a speed as close as possible to drive tape at exactly 10 ips. Lesser brilliance indicates that tape motion will be faster or slower than 10 ips, but still within allowable tolerances.

i. Set tester ON LINE/OFF LINE switch to OFF LINE and check that tester 10 IPS ADJ indicator lamp is blinking. Indicator lamp should be on more than 50% of the time. If not proceed to step o.

j. Set tester ON LINE/OFF LINE switch to OFF.

k. Remove Checkout Cartridge from UNIT 0 CTU Transport Assembly and insert it in UNIT 1.

l. Set tester UNIT switch to 1.

m. Set tester ON LINE/OFF LINE switch to OFF LINE and check that tester 10 IPS ADJ indicator lamp is blinking. Indicator lamp should be on more than 50% of the time. If not proceed to step o.

n. If 10 IPS ADJ indicator lamp indications are as stated in steps i and m, no further adjustment is required. Skip to step q.

o. If tester 10 IPS ADJ indicator lamp indication is erroneous for either CTU Transport Assembly, insert Checkout Cartridge in defective CTU Transport Assembly, set tester UNIT switch to applicable unit number (0 or 1), and slowly adjust Read/Write PCA SPEED potentiometer R55 until tester 10 IPS ADJ indicator lamp is blinking on for more than 50% of the time.

p. Reinsert Checkout Cartridge in remaining CTU Transport Assembly, set tester UNIT switch to applicable unit number, and check that tester 10 IPS ADJ indicator lamp is blinking on for more than 50% of the time. If not, repeat steps o and p until tester 10 IPS ADJ indicator lamp indications are correct. If 10 IPS ADJ indicator lamp indications are correct, no further adjustment is required.

q. Set rear panel AC POWER switch to OFF and remove Checkout Cartridge from terminal.

r. Remove CTU Tester from CTU Interface and Read/Write PCA's and reinstall CTU Top Plane Assembly on top connectors of CTU Interface and Read/Write PCA's.

s. Close terminal mainframe.

3-15. PREVENTIVE MAINTENANCE

3-16. MAGNETIC HEAD CLEANING PROCEDURES

The CTU Transport Assembly magnetic heads should be cleaned after every 50 hours of operation or whenever dust or dirt is detected on the head surfaces. (Location of the magnetic head is illustrated in figure 4-2.) Clean the magnetic heads as follows:

a. Open terminal to its half open position in accordance with paragraph 1-2.

CAUTION

Do not attempt to clean magnetic heads with any cleaning materials other than those provided. Use of solvents other than Freon or alcohol may damage heads. Use of abrasive type cleaners may scratch head surfaces.

b. Saturate cleaning swab with cleaning solvent.

c. Using right-to-left and left-to-right motion, carefully wipe magnetic head surface clean with saturated swab. Do not clean head surface with an up and down motion.

d. Using a clean, dry, cleaning swab, carefully wipe magnetic head surface dry. Do not dry head surface with an up and down motion.

e. Firmly grasp mainframe top cover in one hand and release safety latch by pressing it inboard with other hand. Then, using both hands, carefully lower top cover to its closed position.

3-17. MAGNETIC HEAD DEGAUSSING PROCEDURES

The CTU Transport Assembly magnetic head should be degaussed whenever the magnetic head is suspected of being accidently gaussed by exposure to a high magnetic field. The degaussing procedure requires the use of an HP Hand-held Degausser, part no. 9160-0023 or equivalent. (Location of the magnetic head is illustrated in figure 4-2.) Degauss the magnetic head as follows:

a. Open the terminal to its half open position in accordance with paragraph 1-2.

CAUTION

Remove all tape cartridges from vicinity of degausser.

CAUTION

The degausser should not be left energized for more than five minutes at a time to prevent permanent damage to degausser. Also, ensure that tip of degausser is clean and free of any small bits of metal that might scratch the magnetic head surface.

b. Connect the degausser to an ac power source.

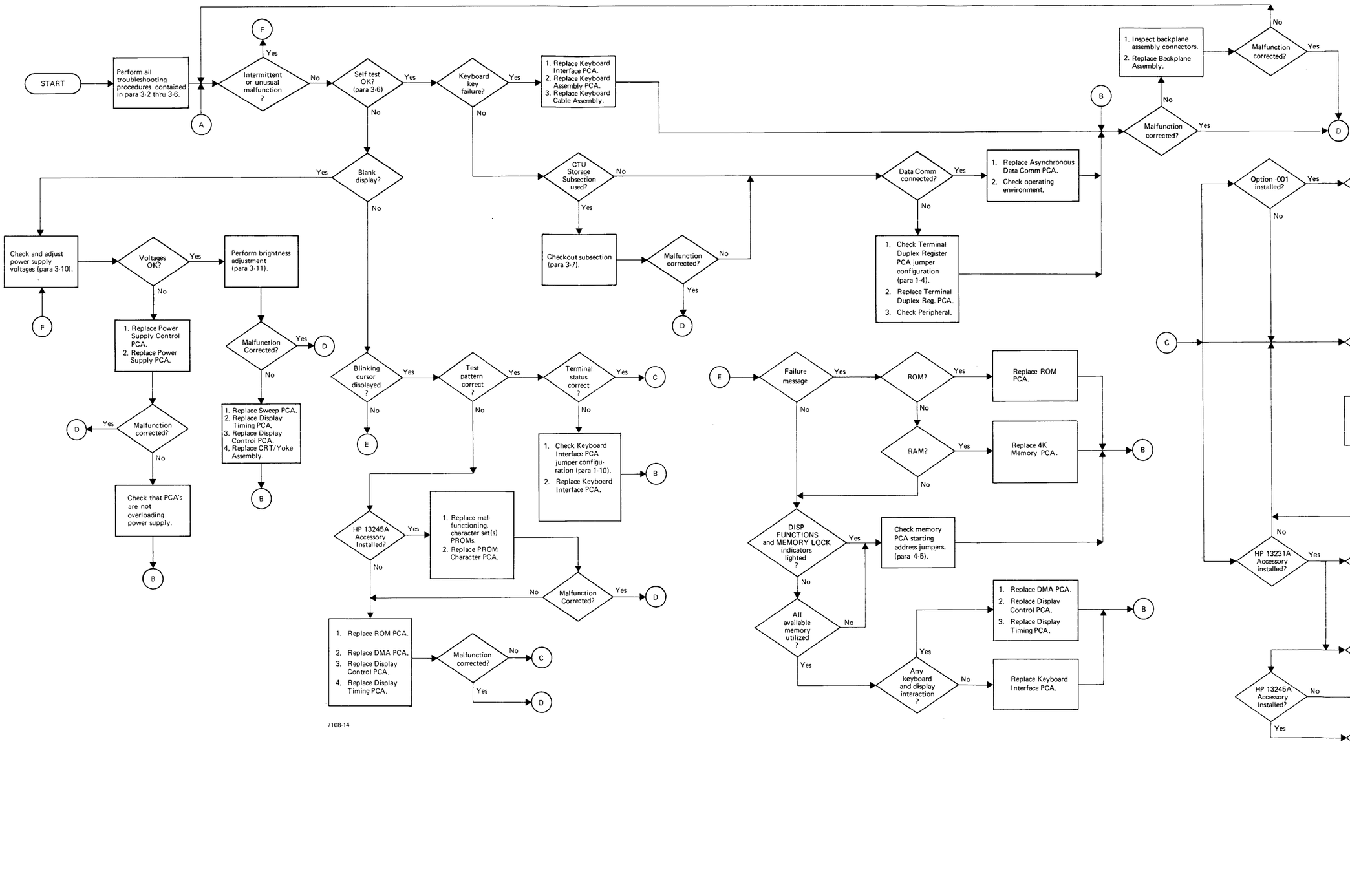
c. Starting from at least three feet away, point tip of degausser toward magnetic head front center surface and slowly approach magnetic head until tip of degausser touches head front center surface.

d. Slowly retract tip of degausser from magnetic head to a distance of at least three feet and disconnect degausser.

e. Firmly grasp mainframe top cover in one hand and release safety latch by pressing it inboard with other hand. Then, using both hands, carefully lower top cover to its closed position.

3-18. TAPE CONDITIONING

Conditioning a tape restores proper tape tension by winding the tape forward to end-of-tape at 60 ips and then rewinding it back to beginning-of-tape at 60 ips. A tape should be conditioned whenever a tape cartridge has been rethreaded, been subjected to sudden environmental changes, or whenever improper tape tension is suspected. To condition a tape, insert the tape cartridge in UNIT 0 CTU Transport Assembly, press and hold down CNTL key, and press TEST key. The UNIT 0 eject button will light, indicating that the tape is in motion and being conditioned. When the cursor replaces the SEARCHING message, tape conditioning is complete. Usually, one tape conditioning sequence is sufficient to restore proper tape tension. The sequence can, however, be repeated as many times as desired. If three conditioning sequences fail to restore proper tape tension, replace tape cartridge.


START
Perform all troubleshooting procedures contained in para 3-2 thru 3-6.
Intermittent or unusual malfunction ?
Yes
No
F
A
Self test OK? (para 3-6)
Yes
No
Keyboard key failure?
Yes
No
1. Replace Keyboard Interface PCA.
2. Replace Keyboard Assembly PCA.
3. Replace Keyboard Cable Assembly.
Blank display?
Yes
No
Check and adjust power supply voltages (para 3-10).
Voltages OK?
Yes
No
Perform brightness adjustment (para 3-11).
1. Replace Power Supply Control PCA.
2. Replace Power Supply PCA.
Malfunction Corrected?
Yes
No
D
1. Replace Sweep PCA.
2. Replace Display Timing PCA.
3. Replace Display Control PCA.
4. Replace CRT/Yoke Assembly.
Malfunction corrected?
Yes
No
D
Check that PCA's are not overloading power supply.
B
Blinking cursor displayed ?
Yes
No
E
Test pattern correct ?
Yes
No
Terminal status correct ?
Yes
No
C
1. Check Keyboard Interface PCA jumper configuration (para 1-10).
2. Replace Keyboard Interface PCA.
B
HP 13245A Accessory Installed?
Yes
No
1. Replace malfunctioning character set(s) PROMs.
2. Replace PROM Character PCA.
Malfunction Corrected?
Yes
No
D
1. Replace ROM PCA.
2. Replace DMA PCA.
3. Replace Display Control PCA.
4. Replace Display Timing PCA.
Malfunction corrected?
No
C
Yes
D
CTU Storage Subsection used?
No
Yes
Checkout subsection (para 3-7).
Malfunction corrected?
No
Yes
D
Data Comm connected?
Yes
No
1. Replace Asynchronous Data Comm PCA.
2. Check operating environment.
1. Check Terminal Duplex Register PCA jumper configuration (para 1-4).
2. Replace Terminal Duplex Reg. PCA.
3. Check Peripheral.
E
Failure message
Yes
No
ROM?
Yes
No
Replace ROM PCA.
RAM?
Yes
No
Replace 4K Memory PCA.
B
DISP FUNCTIONS and MEMORY LOCK indicators lighted ?
Yes
No
Check memory PCA starting address jumpers. (para 4-5).
All available memory utilized ?
No
Yes
1. Replace DMA PCA.
2. Replace Display Control PCA.
3. Replace Display Timing PCA.
B
Any keyboard and display interaction ?
Yes
No
Replace Keyboard Interface PCA.
1. Inspect backplane assembly connectors.
2. Replace Backplane Assembly.
Malfunction corrected?
No
Yes
B
Malfunction corrected?
No
Yes
D
Option -001 installed?
Yes
No
C
HP 13231A Accessory installed?
Yes
No
HP 13245A Accessory Installed?
No
Yes

7108-14

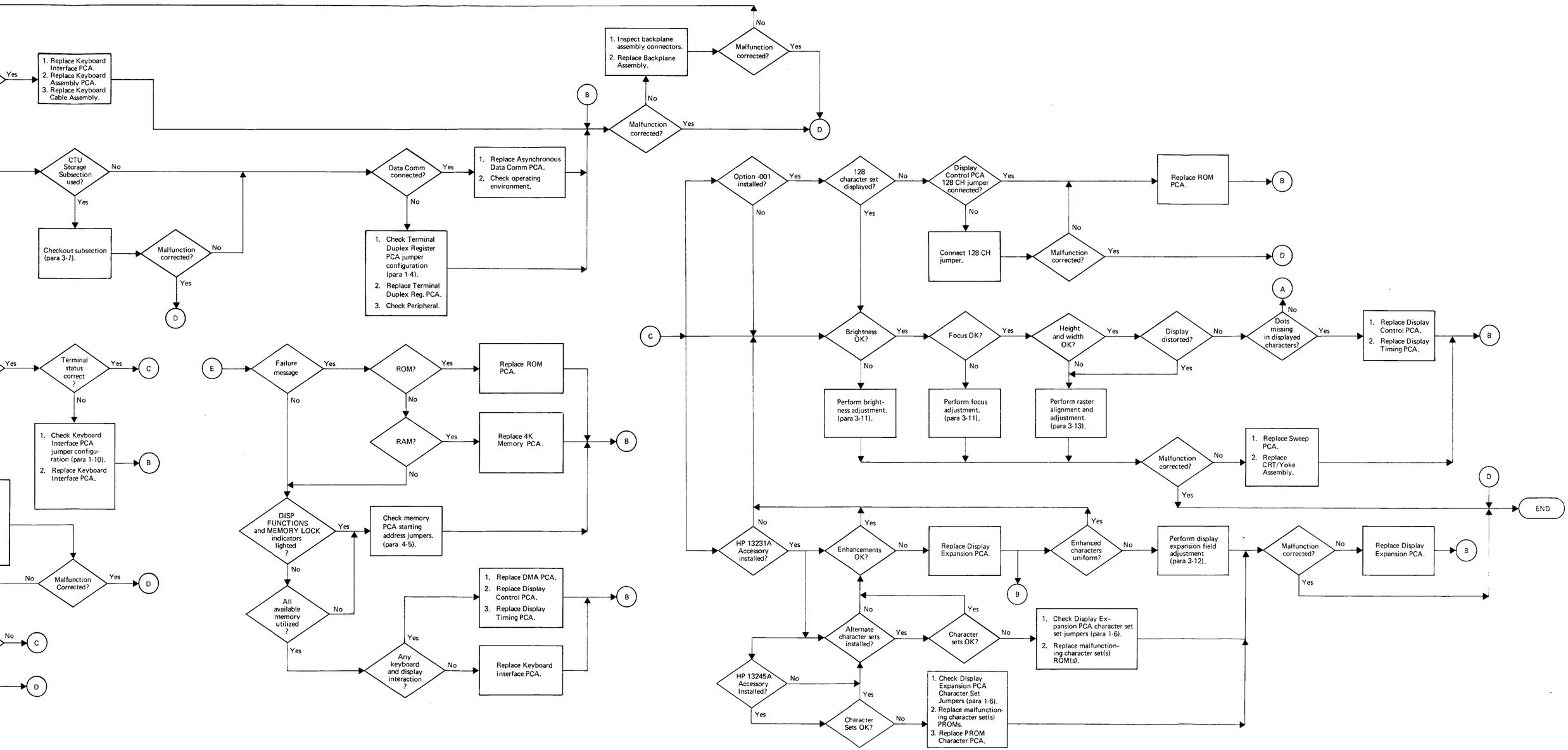
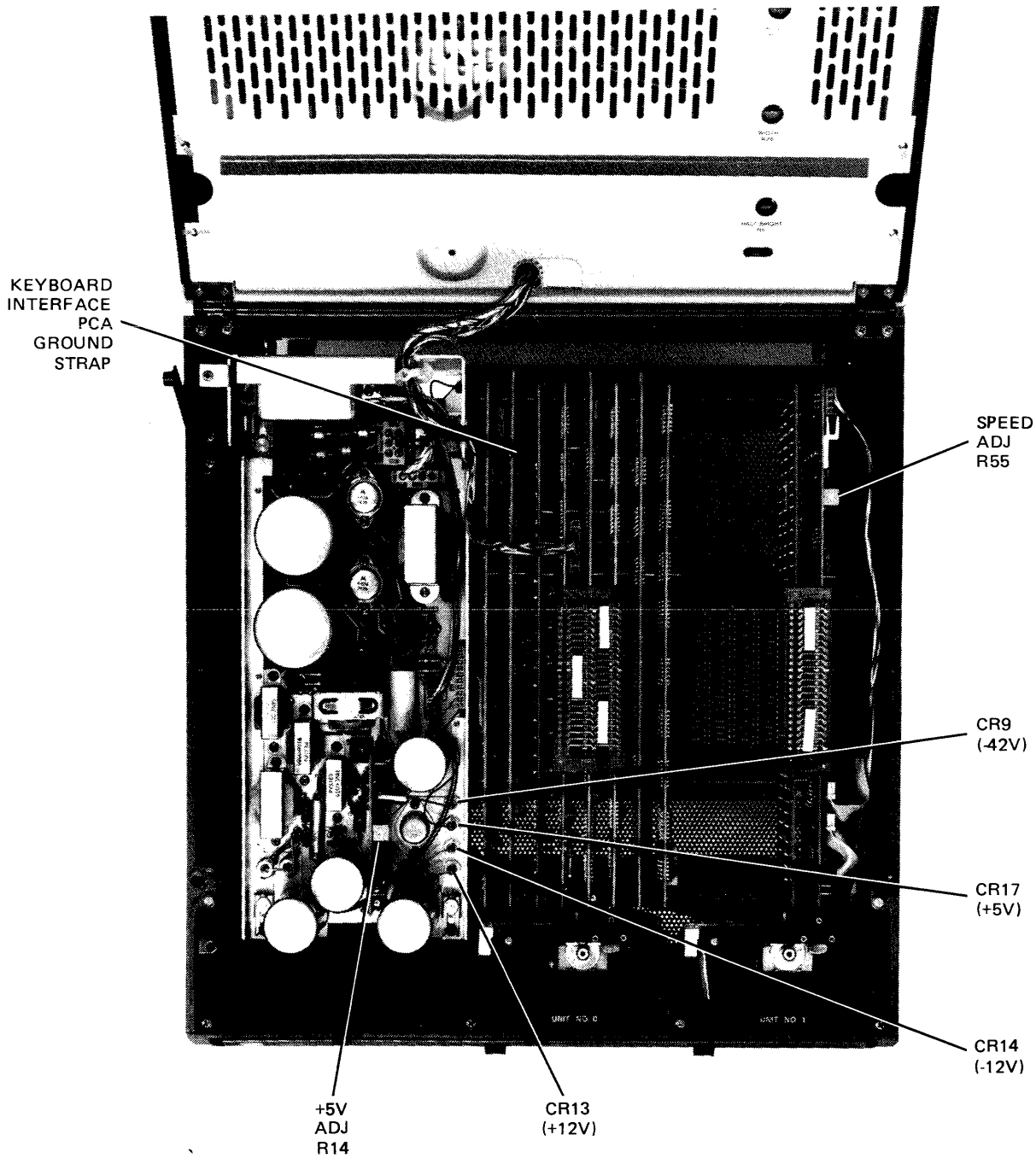
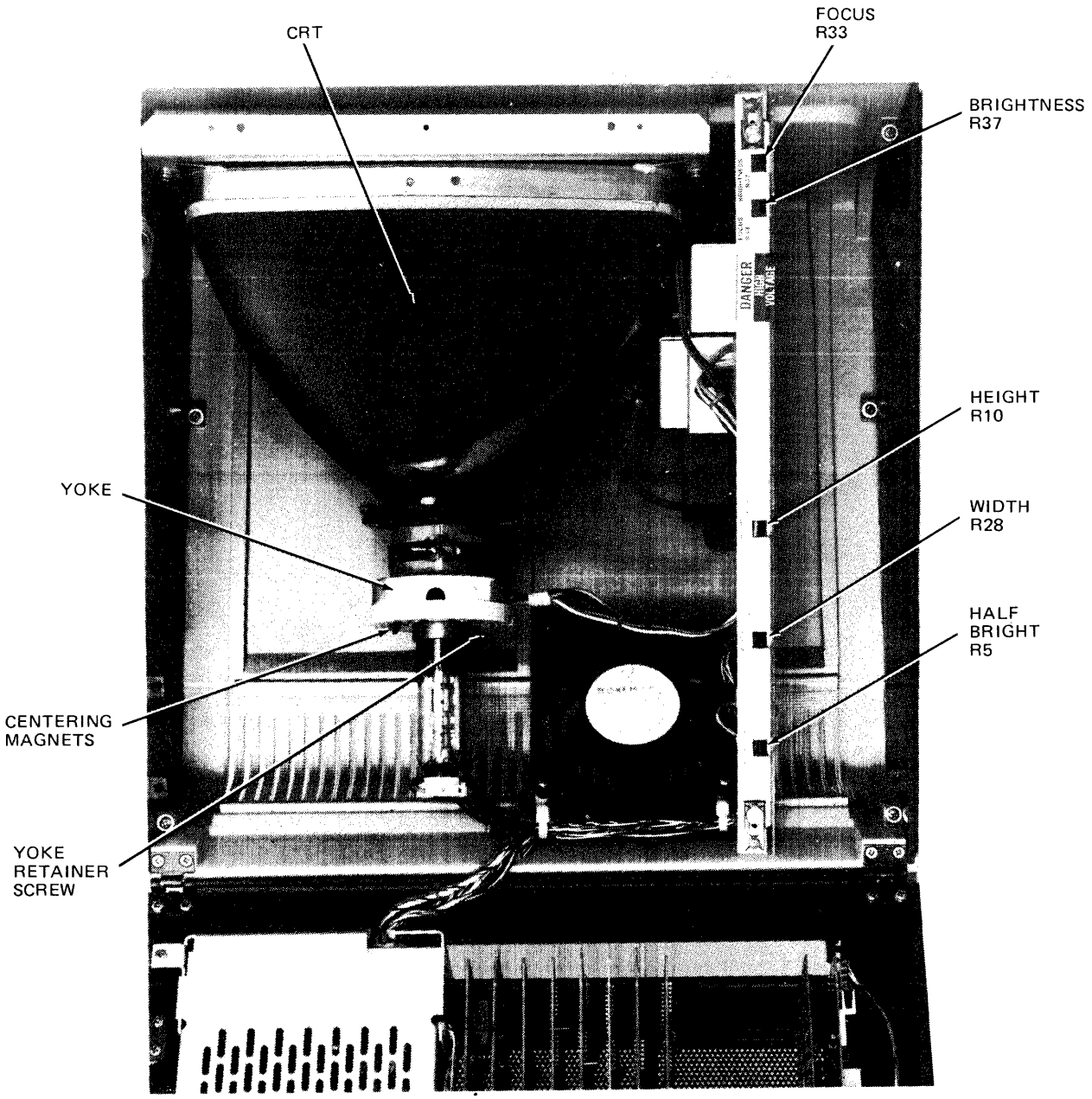


Figure 3-1. Troubleshooting Flowchart



7108-12

Figure 3-2. Mainframe Bottom Test Point and Adjustment Locations



7108-13

Figure 3-3. Mainframe Top Adjustment Locations

3-19. USING THE HP CTU TESTER

The HP CTU Tester, part no. 02640-60082 is used in place of the CTU Top Plane Assembly to provide visual displays for troubleshooting and adjusting the storage subsection and to provide optional local control of CTU tape motion.

3-20. CONTROLS AND INDICATORS

The CTU Tester controls and indicators are shown in figure 3-4 and described in table 3-3. Each control and indicator listed in table 3-3 is referenced by index number to figure 3-4 for ease of identification.

3-21. INSTALLING THE TESTER

Install the CTU Tester in place of the terminal CTU Top Plane Assembly as follows:

a. Open terminal to its half open position in accordance with paragraph 1-2.

b. Insert connector removal tool under CTU Top Plane Assembly (figure 1-1) and remove assembly by pressing down on removal tool handle. (Use of the connector removal tool is shown in figure 1-5.)

c. Install CTU Tester on CTU Interface and Read/Write PCA top connectors so that tester display indicator lamps are closest to rear of terminal mainframe.

d. Set tester ON LINE/OFF/OFF LINE switch to OFF.

e. Reconnect power cord to mainframe rear panel LINE connector.

f. Set rear panel AC POWER switch to on position.

3-22. TROUBLESHOOTING WITH THE TESTER

3-23. TROUBLESHOOTING PHILOSOPHY. Before attempting to use the tester as a troubleshooting device, it is imperative to understand what each tester display indicator lamp signifies and which storage subsection circuits are associated with each indicator lamp. Use table 3-3, paragraphs 2-30 through 2-33, and figure 2-2 for reference.

Once familiar with the tester displays and storage subsection circuits, two other important facts must be understood: 1) when using the tester on line, the display indicator lamps are monitoring the signal paths between the CTU Interface PCA and Read/Write PCA just as though the CTU Top Plane Assembly was installed, and; 2) when using the tester off line, the CTU Interface PCA is isolated from the rest of the subsection and the tester indicator lamps are monitoring the signal paths between the tester and Read/Write PCA. Therefore, if a specific malfunction is indicated during on line testing, but is not indicated during off line testing, it is most probable that the trouble exists in the CTU Interface PCA circuits, assuming that the basic terminal is operating properly. Conversely, if the same malfunction is indicated during both on line and off line testing, it is most probable that the trouble exists in either the Read/Write PCA or the CTU Transport Assemblies.

Once a trouble is isolated to either the Read/Write PCA or the CTU Transport Assemblies, it should be remembered that the CTU Transport Assemblies share common read, write, and tape motion circuits on the Read/Write PCA. Therefore, if a specific malfunction is indicated for UNIT $\emptyset$, but is not indicated for UNIT 1, it is most probable that the trouble exists in the UNIT $\emptyset$ CTU Transport Assembly. Conversely, if the same malfunction is indicated for both UNIT $\emptyset$ and UNIT 1, it is most probable that the trouble exists in the Read/Write PCA circuits.

3-24. TROUBLESHOOTING PROCEDURE. When a malfunction has occurred in the storage subsection that cannot be quickly isolated using the checkout procedures in paragraph 3-7, continue to troubleshoot with the tester as follows:

a. Install the tester in accordance with paragraph 3-21.

b. Set tester ON LINE/OFF/OFF LINE switch to ON LINE.

c. Repeat checkout procedure in accordance with paragraph 3-7 while observing tester display indicator lamps.

d. When the malfunction occurs, compare its symptoms against the tester display indicator lamps. In some cases, the malfunction can be isolated at this point. For example; if a NO TAPE message is displayed and the tester CRTG IN indicator lamp is lighted for the selected CTU Transport Assembly, it is most probable that the trouble exists in the CTU Interface PCA because the lighted CRTG IN indicator lamp verifies that the CTU Transport Assembly and Read/Write PCA cartridge detect circuits are operating properly.

e. If the malfunction cannot be isolated by performing the previous step, set tester ON LINE/OFF/OFF LINE switch to OFF, determine how to duplicate the operation where the malfunction occurred with the tester, set tester control switches to required positions, set ON LINE/OFF/OFF LINE switch to OFF LINE, and again check the malfunction symptoms against the tester display indicator lamps. If the malfunction no longer exists, it is mot probable that the trouble exists in the CTU Interface PCA circuits. If the malfunction still exists, it is most probable that the trouble exists in either the Read/Write PCA or selected CTU Transport Assembly circuits. For example; if READ FAIL or END OF DATA message is repeatedly displayed and the malfunction cannot be isolated by performing step d, set tester ON LINE/OFF/OFF LINE switch to OFF and duplicate a read operation as follows:

   (1) Insert a prerecorded tape in CTU Transport Assembly that was being tested when the malfunction occurred.

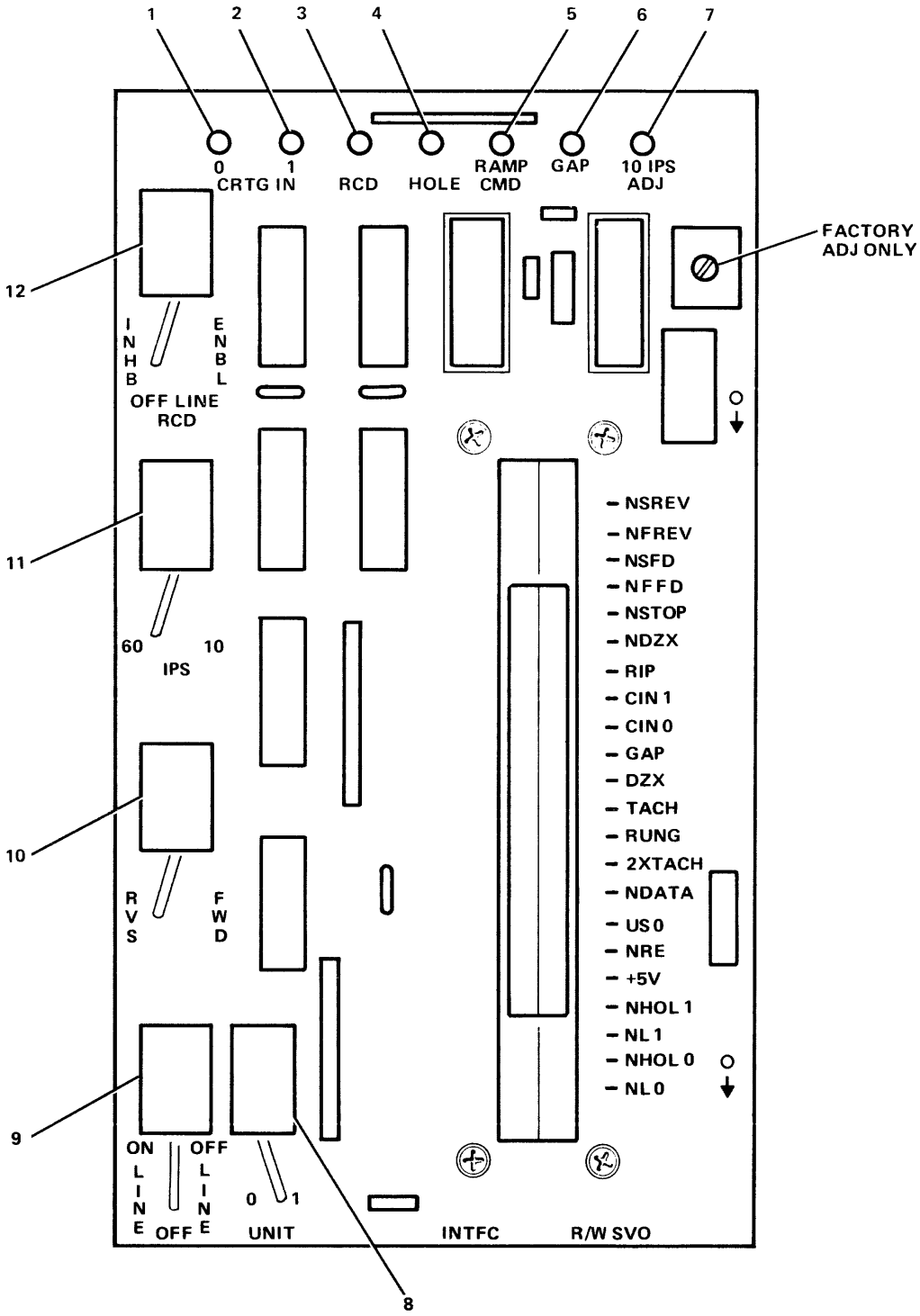


Figure 3-4. CTU Tester Controls and Indicators

Table 3-3. CTU Tester Controls and Indicators

INDEX NO.	NOMENCLATURE	DESCRIPTION
1	CRTG IN 0 indicator	When lighted, indicates that a tape cartridge is inserted in UNIT 0 CTU Transport Assy. Also verifies proper operation of UNIT 0 Head Bridge Assy switch circuit and Read/Write PCA cartridge detect circuit.
2	CRTG IN 1 indicator	When lighted, indicates that a tape cartridge is inserted in UNIT 1 CTU Transport Assy. Also verifies proper operation of UNIT 1 Head Bridge Assy switch circuit and Read/Write PCA cartridge detect circuit.
3	RCD indicator	When lighted, indicates that data is being recorded on selected CTU Transport Assy tape. Also verifies proper operation of Read/Write PCA write current circuit when tester is in ON LINE mode.
4	HOLE indicator	When lighted, indicates that a hole is being detected in selected CTU Transport Assy tape. Also verifies proper operation of Head Bridge Assy hole detection circuit.
5	RAMP CMD indicator	When lighted, indicates that a tape motion signal is being generated. Also verifies proper operation of Read/Write PCA CTU drive circuits. Also verifies CTU Interface PCA tape motion decoder and command logic when tester is used in ON LINE mode.
6	GAP indicator	When blinking, indicates that tape containing recorded data is moving past selected CTU Transport Assy magnetic head. Also verifies proper operation of Head Bridge Assy magnetic head and Read/Write PCA unit/function decoder, read select switch, read amplifier circuit, and gap detect circuit. Lamp on indicates presence of inter-record gap.
7	10 IPS ADJ indicator	When on, indicates that selected CTU Transport Assy is driving tape at 10 ips ±1.0%. Also verifies proper operation of CTU Transport Assy Motor/ Tachometer Assy; Read/Write PCA amplifier select logic, CTU drive circuits, tachometer feedback select and conditioning circuits, and feedback circuit; and CTU Interface PCA command logic and tape motion decoder.
8	UNIT switch	When operating OFF LINE, selects either UNIT 0 or UNIT 1 CTU Transport Assy and lights eject button of selected unit. Also verifies proper operation of Head Bridge Assy indicator lamp circuit and Read/Write PCA amplifier select logic and unit/function decoder.
9	ON LINE/OFF/ OFF LINE switch	When set to ON LINE, CTU Tester performs as a CTU Top Plane Assy with visual displays. Storage subsection is controlled by terminal keyboard and CTU Interface PCA. When set to OFF LINE, storage subsection is controlled by CTU Tester, CTU Interface PCA is disabled, and tape motion is determined by RVS/FWD and IPS switches. Tape motion will stop when a hole is detected. When set to OFF, all tape motion and control is inhibited; CTU Tester and CTU Interface PCA are both disabled.
10	RVS/FWD switch	When operating OFF LINE, controls tape motion direction (reverse or forward) for CTU Transport Assy selected by UNIT switch. Verifies proper operation of Read/Write PCA CTU drive circuits, for both tape directions.

Table 3-3. CTU Tester Controls and Indicators (Cont)

INDEX NO.	NOMENCLATURE	DESCRIPTION
11	IPS switch	When operating OFF LINE, controls tape speed (60 or 10 ips) for CTU Transport Assy selected by UNIT switch. Also verifies proper operation of same circuits as RVS/FWD switch.
12	OFF LINE RCD switch	When operating OFF LINE and set to INHB, enables read mode circuits. When operating OFF LINE and set to ENBL, enables write mode circuits. Also verifies proper operation of Head Bridge Assy magnetic head and Read/Write PCA unit/function decoder, read select switch, read amplifier circuit, and gap detect circuit.

(2) Set tester UNIT switch to corresponding number of CTU Transport Assembly under test.

(3) Set tester OFF LINE RCD switch to INHB, IPS switch to 10, and RVS/FWD switch to FWD.

CAUTION

The tester does contain "stop on hole detect" circuitry. However, to ensure prevention of tape run-off, it is recommended to discontinue tape motion commands once a "hole detect" has stopped the tape.

CAUTION

To restart tape motion, ON LINE/OFF/OFF LINE switch must first be set to OFF and then back to OFF LINE. However, care should be taken to change direction of tape motion to prevent tape run-off.

(4) Set tester ON LINE/OFF/OFF LINE switch to OFF LINE and observe GAP indicator lamp. If GAP indicator lamp is blinking, it is most probable that the trouble exists in the CTU Interface PCA because the blinking GAP indicator lamp verifies that the CTU Transport Assembly and most of the Read/Write PCA read circuits are operating properly. If the GAP indicator lamp is not blinking, it is most probable that the trouble exists in either the CTU transport Assembly or the Read/Write PCA. Set tester ON LINE/OFF/OFF LINE switch to OFF, insert prerecorded tape in other CTU Transport Assembly, set ON LINE/OFF/OFF LINE switch to OFF LINE, and again observe the GAP indicator lamp. If the GAP indicator lamp is blinking, it is most probable that the trouble exists in the CTU Transport Assembly originally under test. If the GAP indicator is not blinking, it is most probable that the trouble exists in the Read/Write PCA read circuits commonly shared by both CTU Transport Assemblies.

f. Once the malfunction has been isolated, perform the necessary repair procedures and repeat steps a, b, and c to ensure that the storage subsection is now operating properly.

g. Remove tester from terminal and reinstall CTU Top Plane Assembly on CTU Interface PCA and Read/Write PCA top connectors.

h. Firmly grasp mainframe top cover in one hand and release safety latch by pressing it inboard with other hand. Then, using both hands, carefully lower top cover to its closed position.

REPAIR

SECTION IV

4-1. INTRODUCTION

This section contains instructions for removing and replacing mini data station (terminal) assemblies, instructions for rethreading a tape cartridge, and a listing of field-replaceable parts.

WARNING

Hazardous voltages are present inside equipment. The procedures contained in this section shall be performed only by qualified service personnel.

VORSICHT

Innerhalb des Geräts bestehen gefährliche Spannungen. Die in diesem Abschnitt enthaltenen Arbeiten dürfen nur durch Betriebsfachpersonal durchgeführt werden.

ATTENTION

Des tensions dangereuses sont présentes à l'intérieur du matériel. Les opérations décrites dans cette section ne devront être effectuées que par un personnel qualifié.

AVVISO

Pericolo: Alta tensione presente in questa apparecchiatura. Le procedure contenute in questa sezione debbono essere effettuate soltanto da qualificato personale di servizio.

ADVERTENCIA

Hay voltaje peligroso en el interior de este equipo. Los procedimientos expuestos en esta sección sólo deberá llevarlos a cabo el personal de servicio calificado.

高圧危険

内部装置に危険な高電圧がきています。この章にある処置や手続に関しては、専門のサービスマンによってのみ行なって下さい。

4-2. REMOVAL AND REPLACEMENT

WARNING

Always remove AC power from terminal before attempting any parts replacements. Use extreme caution when working near the CRT, Yoke Cable Assembly, and Sweep PCA high voltage sections.

VORSICHT

Vor Auswechseln von Einzelteilen ist jeweils der Wechselstromanschluss von der Klemme zu trennen. Bei Arbeiten in der Nähe der Hochspannungsteile von Kathodenstrahlröhre (CRT), Joch-Kabelsatz (Yoke Cable Assembly) sowie der gedruckten Schaltung für den Kipposzillator (Sweep PCA) ist grösste Vorsicht zu beachten.

ATTENTION

Toujours couper l'arrivée de courant alternatif des bornes avant d'entreprendre tout remplacement de pièces. Redoubler de prudence lorsqu'on travaille à proximité des sections haute tension du tube cathodique (CRT), de l'ensemble de câbles de culasse (Yoke Cable Assembly), et de l'ensemble de tableau de circuit oscillant (Sweep PCA).

AVVISO

Isolare sempre la tensione c.a. dal morsetto prima di procedere alla sostituzione di qualsiasi parte. Usare estrema cautela durante operazioni in prossimità delle sezioni ad alta tensione del tubo a raggi catodici (CRT), della linea montaggio cavo collegamento (Yoke Cable Assembly), e della linea del circuito stampato per l'oscillatore di base di tempi (Sweep PCA).

ADVERTENCIA

Desconéctese siempre la corriente alterna del terminal antes de intentar reemplazar cualquier pieza. Téngase sumo cuidado ai trabajar cerca de las secciones de alta tensión del tubo de rayos catódicos (CRT), del conjunto de cable de horquilla (Yoke Cable Assembly), y del circuito impreso del oscilador de base de tiempo (Sweep PCA).

⚠ **高圧危険** ⚠

どんな部品でも交換する場合は、その前にＡＣの電源コードを機器よりはずして下さい。ＣＲＴ、ヨーク・ケーブルアセンブリ、スイープＰＣＡなどの高電圧がかかっている部分の近くでは、危険ですから特に注意を払って下さい

Due to the modular design of the terminal, no special instructions are required for removing and replacing parts except for those discussed in paragraphs 4-3 through 4-10. To remove most replaceable parts, first refer to figure 4-1 and the replaceable parts list to determine how the part is attached and the number of attaching parts involved. Once this is accomplished, removal procedures for the part will be obvious. Always disconnect any attached cable assemblies before attempting to remove a part. Replacing a part is simply a matter of reversing the removal procedure.

4-3. DISPLAY CONTROL PCA

The Display Control PCA is manufactured with a jumper installed for use with a 128 character set terminal (Option 001). When replacing the Display Control PCA, first determine whether the terminal is equipped with a 64 character set (standard model) or a 128 character set. For standard model terminals, disconnect the soldered in 128 CH jumper located approximately in the center of the Display Control PCA before installing it in the terminal. For Option 001 terminals, install the PCA in the terminal as shipped from the factory.

4-4. FAN AND CABLE ASSEMBLY

When removing the Fan and Cable Assembly (65, figure 4-4), first open the terminal mainframe to its full open position in accordance with paragraph 1-2. Then, disconnect the assembly's connector from the Power Supply PCA and remove the two cable clamps and wire harness attached to the fan. After removing the assembly's cable from the existing wire harness and cable clamps, remove the four screws and washers (66 and 67) securing the assembly to the mainframe top and remove the assembly from the terminal. Installing the Fan and Cable Assembly is basically accomplished by performing the removal procedures in reverse order. However, care should be taken to ensure that the assembly's cable is secured within the existing wire harness and cable clamps. Also, the assembly must be mounted so that its cable is closest to the back of the mainframe top and CRT, and the fan AIRFLOW arrow must point toward the back of the mainframe top.

4-5. ROM PCA AND +4K MEMORY PCA

No special instructions are required to remove the ROM or +4K Memory PCA's. However, when replacing either PCA, ensure that the replacement PCA jumpers are configured as shown in figure 4-1.

4-6. CARTRIDGE TAPE MODULES

The cartridge tape modules consist of the CTU Interface PCA, Read/Write PCA, and two CTU Transport Assemblies. No special instructions are required to remove these modules except to exercise caution when handling the CTU Transport Assemblies to ensure that the magnetic heads are not damaged. However, before attempting to replace any cartridge tape modules, refer to the detailed installation instructions for the applicable module in paragraph 1-8. It should be noted that when removing the front bezel (15, figure 4-4) to replace a defective CTU Transport Assembly, that the four screws (16) securing the bezel in place should be loosened only to the extent necessary to remove the bezel and should not be completely removed from the bezel. Completely removing the screws (16) may result in damage or loss of the associated o-rings (17). If a malfunction develops in a CTU Transport Assembly, it is recommended that the entire CTU Transport Assembly be replaced rather than replacing a defective transport subassembly. However, if it becomes necessary to disassemble a CTU Transport Assembly, first refer to figure 4-2 and then disassemble the transport in reverse order of the assembly instructions contained in the following paragraph.

Note: The CTU Base Assembly pawl is held in place by spring tension only and is captured when the Head Bridge Assembly is attached to the CTU Base Assembly. Use caution when removing the Head Bridge Assembly to ensure that the pawl is not lost.

If a CTU Transport Assembly has been removed and disassembled, reassemble the three subassemblies as follows:

a. Attach two Capstan Loading Springs (figure 4-2) to Motor/Tachometer Assembly casting as shown in figure 4-2.

b. Set Motor/Tachometer Assembly into CTU Base Assembly Ball Sockets and, using a pair of long-nose pliers or equivalent, attach loose ends of Capstan Loading Springs to CTU Base Assembly.

c. Set Pawl in CTU Base Assembly Pawl Pocket and carefully secure Pawl in Pawl Pocket by placing end of Torsion Spring behind Pawl.

d. Using two alignment pins and sockets, carefully place Head Bridge Assembly on top of CTU Base Assembly and capture Pawl.

e. Partially secure Head Bridge Assembly to CTU Base Assembly with one screw and washer at left, rear of Head Bridge Assembly behind captured Pawl.

f. Install Compression Spring on CTU Base Assembly and capture Compression Spring in place with Head Bridge Assembly.

g. Secure Head Bridge Assembly in place with remaining two screws and washers.

h. Loosen and retighten screw securing left, rear of Head Bridge Assembly.

i. Connect Tachometer Cable connector to Head Bridge Assembly Connector P1.

j. Install reassembled CTU Transport Assembly in terminal in accordance with paragraph 1-8.

4-7. POWER SUPPLY CONTROL, POWER SUPPLY, AND SWEEP PCA'S

In addition to its mating connector, the Power Supply Control PCA (2, figure 4-4) is attached to the Power Supply PCA (3) with two slotted PCA mounting guide posts that contain detents to lock the PCA in place. To remove the Power Supply Control PCA, first pull one of the mounting guide posts slightly away from the PCA's edge to free the detent and then, carefully rock the PCA up and out of its mating connector on the Power Supply PCA. To replace the PCA, align the PCA's edges with the mounting guide post slots and press down firmly on the PCA until it is seated in its mating connector and locked in place by the mounting guide post slot detents.

To remove the Power Supply PCA (3, figure 4-4), first remove the power supply housing (1) by unlatching the two snap locks on front of housing and pulling the housing up and out toward the front of the mainframe shell (51). Then, after disconnecting the three wire harness connectors from the PCA, unlatch the snap locks in each of the four corners of the PCA and lift the entire PCA up and out of the mainframe shell. Installing the Power Supply PCA is basically accomplished by performing the removal procedures in reverse order. However, care should be taken not to damage the Backplane Assembly (44) connector pins that mate with the Power Supply PCA bottom connector J2.

To remove the Sweep PCA (63, figure 4-4), first open the terminal mainframe to its full open position in accordance with paragraph 1-2. Then, unlatch the snap locks at each end of the Sweep PCA and move the PCA up and to the right far enough to gain easy access to all cable connectors. Disconnect the High Voltage Cable Assembly from the CRT by pressing the cable assembly connector sides together and pulling it out of the CRT. Disconnect the remaining four cable connectors from the Sweep PCA and completely remove the PCA from the terminal. It is recommended that the cable connectors be disconnected in the order of P1, P2, P4, and P3.

4-8. ACCESSORIES

No special instructions are required to remove any terminal accessories. However, before attempting to replace an accessory, refer to the detailed installation instructions for the applicable accessory in Section I of this manual.

4-9. PROM CHARACTER PCA

The PROM Character PCA consists entirely of field replaceable parts. After removing the PCA from the terminal, refer to figure 4-5 for component location and identification information.

4-10. KEYBOARD OVERLAY AND KEYBOARD

The keyboard overlay (70, figure 4-4) is tension mounted on the keyboard top (72) by means of the overlay's hooked left end and a tension spring attached under its right end. To remove and replace the overlay, proceed as follows:

a. Locate keyway on right side of keyboard top and insert access key supplied with terminal.

b. Push access key into keyway (no key rotation is required) until overlay tension spring is released.

c. When the tension spring is released, the right end of the overlay should raise up high enough to grasp. If not, the right end of the overlay can be pried up with a small screwdriver or similar tool.

d. Unhook the left end of the overlay from the keyboard top by sliding it up and to the left and remove overlay from keyboard top.

e. When replacing the overlay, hook the left end of the overlay in place on the keyboard top, guide the overlay down over the switch keys, and press down on the right end of the overlay until the tension spring snaps into place.

The keyboard is disassembled by removing five screws (80, figure 4-4) and ten washers (81 and 82) from keyboard bottom (89), and lifting off keyboard top (79). After keyboard top is off, the Keyboard Assembly (83) can be removed by disconnecting it from the two Keyboard Cable Assembly (72) connectors and Loudspeaker Assembly (78), and lifting it out of the keyboard bottom.

4-11. TAPE CARTRIDGE RETHREADING

Tape rethreading is difficult and is not recommended unless the data recorded on the runoff tape must be recovered. Instead, when tape runoff occurs, it is recommended to replace the entire tape cartridge. The rethreading procedures contained in this paragraph are for rethreading tape onto the tape cartridge's left tape hub. If a tape run-off condition occurs from the right tape hub, use the left tape hub rethreading instructions except interchange all right-hand and left-hand instructions and change all counter-clockwise directions to clockwise directions. This procedure requires the use of a small Phillips-head screwdriver. Rethread tape onto the left tape hub as follows:

CAUTION

Whenever the tape cartridge top cover is removed, the spring-loaded door and spring can easily slide off the door pivot post. To prevent loss of parts, ensure that door is always completely seated on its pivot post as long as the tape cartridge top cover and backplate are separated.

a. Remove tape cartridge top cover by removing four screws from backplate with Phillips-head screwdriver.

b. As shown in figure 4-3, view A, rethread loose end of tape around right tape guide, through tape cleaner, past belt drive puck, outside guide pin, and around left tape guide so that approximately 1-3/4 inches of tape is clear of guide.

c. Hold tape cartridge as shown in figure 4-3, view B, so that right hand can be used to rotate belt drive puck and left hand can be used to maintain tape tension at left tape guide.

d. Moisten inside surface of free end of tape and, while maintaining tape tension at left tape guide, rotate belt drive puck counterclockwise to wrap free end of tape around left tape hub until tape reaches point where drive belt touches tape hub.

e. While maintaining tape tension, use any small round-tipped tool to trap free end of tape between drive belt and left tape hub as shown in figure 4-3, view C.

f. Rotate belt drive puck counterclockwise until tape is wrapped several times around left tape hub past first set of tape holes (approximately two feet).

g. Replace tape cartridge top cover on backplate and secure in place with four screws.

h. Condition tape in accordance with the instructions contained in Section III.

4-12. REPLACEABLE PARTS

Replaceable parts for the terminal are listed in tables 4-1 and 4-2. The replaceable parts in table 4-1 are referenced to the exploded view (figure 4-4) of the terminal by index numbers which are in disassembly order, except attaching parts are listed immediately after the parts they attach. Items in the DESCRIPTION column of table 4-1 are indented to indicate item relationship. In addition, the symbol "— — — X — — —" follows the last of one or more attaching parts. Indention is as follows:

MAJOR ASSEMBLY

· Replaceable Assembly

· Attaching Parts for Replaceable Assembly

·· Subassembly Parts

·· Attaching Parts for Subassembly Parts

Table 4-1 provides the following information for each part:

a. FIG & INDEX NO. The figure and index where the replaceable parts are shown in the exploded view.

b. HP PART NO. The Hewlett-Packard part number for each replaceable part.

c. DESCRIPTION. The description and any special applications (accessories and options) for each replaceable part.

d. UNITS PER ASSY. The total quantity of each part used in the major assembly.

Table 4-2 provides the reference designation, Hewlett-Packard part number, and description for each PROM Character PCA replaceable part. In addition, table 4-2 provides the original manufacturer's part number for each replaceable part and a manufacturer code number which is cross-referenced to the code list of manufacturers contained in table 4-3. Table 4-3 contains each manufacturer's name, address, and code number. The code numbers are from the *Federal Supply Code for Manufacturers Cataloging Handbooks H4-1* and *H4-2*, and the latest supplements.

4-13. ORDERING INFORMATION

To order replaceable parts for the terminal or options and accessories, address the order to the local Hewlett-Packard Sales and Service Office listed at the end of this manual. The following information should be included in the order for each part.

a. Complete terminal model number (including options and accessories) and serial number.

b. Hewlett-Packard part number.

c. Complete part description as provided in the replaceable parts list.

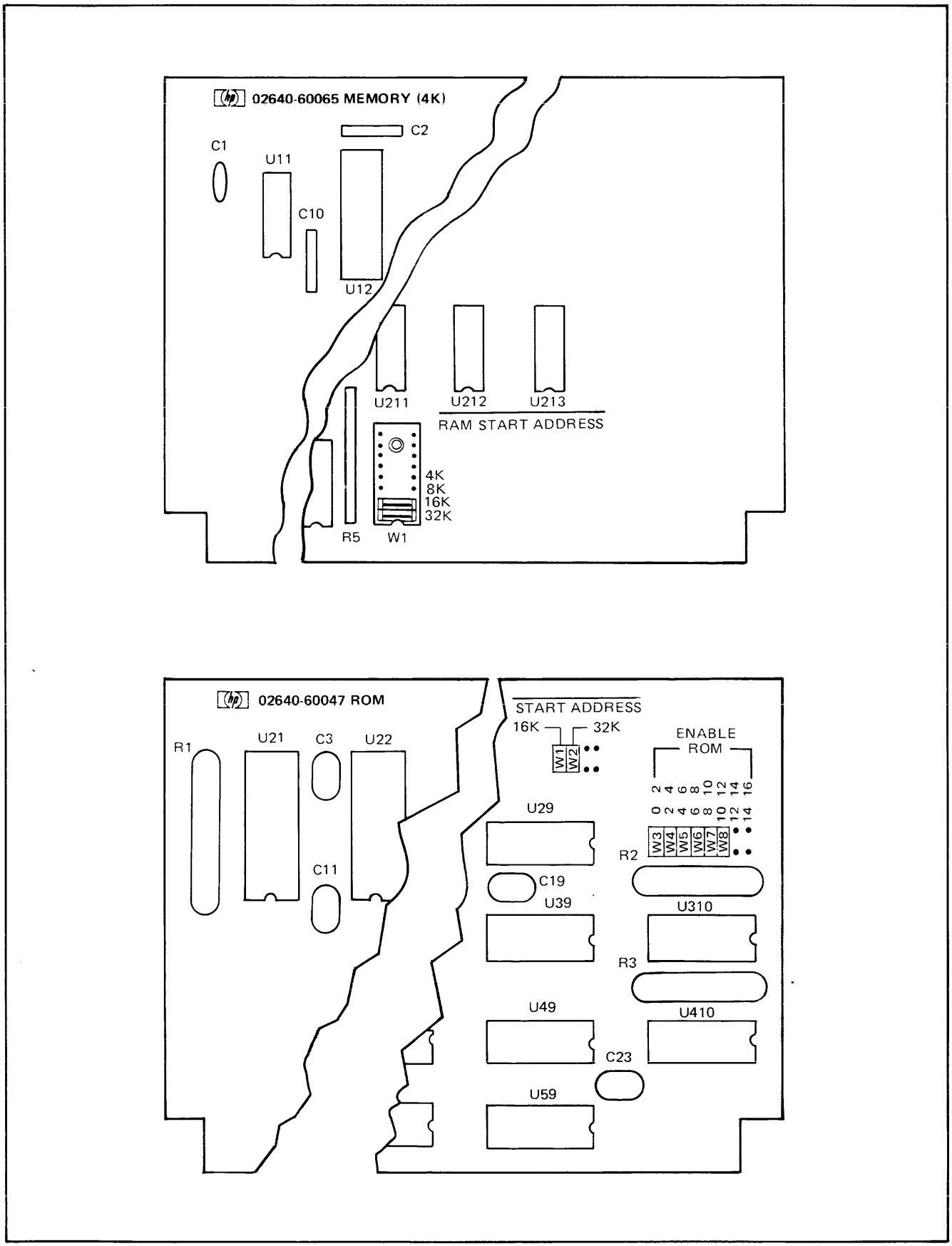


Figure 4-1. ROM PCA and +4K Memory PCA Jumper Configurations

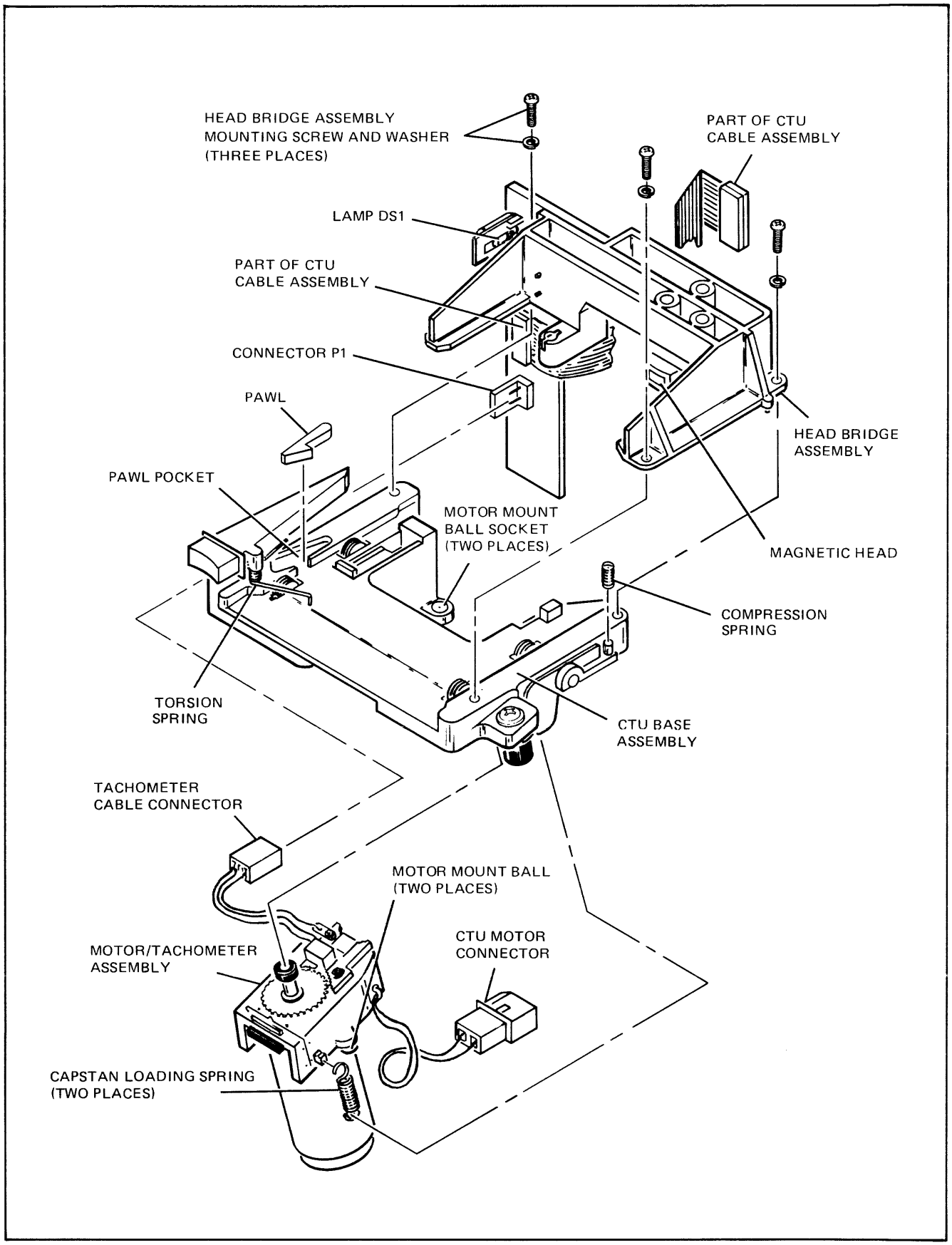


Figure 4-2. CTU Transport Assembly, Exploded View

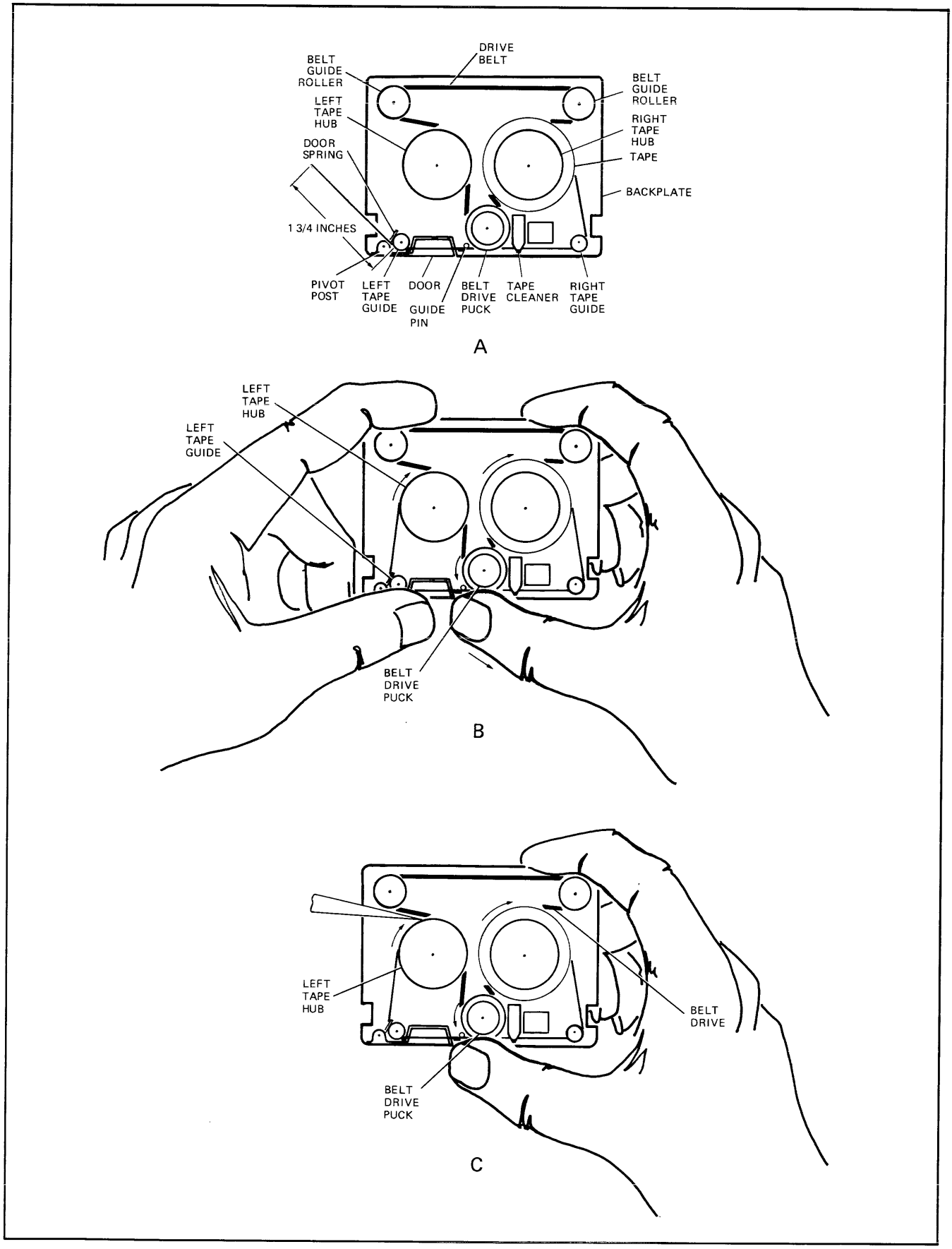


Figure 4-3. Tape Cartridge Rethreading

Table 4-1. Terminal Replaceable Parts List (Sheet 1 of 6)

FIG. & INDEX NO.	HP PART NO.	DESCRIPTION	UNITS PER ASSY.
4-4-	2644A	Mini Data Station	
1	02640-00001	• Housing	1
2	02640-60029	• Power Supply Control Assembly	1
3	02640-60004	• Power Supply Assembly	1
4	8120-1378	• Power Cord Set, 250V, 6A	1
	8120-1351	• Power Cord Set, 250V, 13A	1
	8120-1369	• Power Cord Set, 250V, 10A	1
	8120-1689	• Power Cord Set, 250V, 10/16A	1
	02640-60027	• Rear Panel Assembly	1
		(Attaching Parts)	
5	2360-0197	• Screw, Machine, ph, no. 6-32, 3/8 in.	2
6	2109-0851	• Washer, Lock, split, no. 6	2
		– – – X – – –	
7	2110-0464	•• Fuseholder Body	1
		(Attaching Parts)	
	1400-0090	•• Washer, Neoprene, 5/8 in. OD	1
	2190-0037	•• Washer, Lock, int-tooth	1
	2950-0054	•• Nut, Hex, 1/2-28	1
		– – – X – – –	
	2110-0465	•• Fuseholder Cap	1
	2110-0365	•• Fuse, 4A, SB, 250V (F1)	1
	2110-0303	•• Fuse, 2A, SB, 250V (F1) (used for Option 015)	1
8	3101-0646	•• Power Switch	1
		(Attaching Parts)	
	0590-0012	•• Nut, Self-locking, knurled, no. 15/32-32	1
	2190-0102	•• Washer, Lock, int-tooth, 7/16 in. ID	1
	2950-0035	•• Nut, Hex, 15/32-32	1
		– – – X – – –	
9	9135-0028	•• Line Filter	1
		(Attaching Parts)	
10	2420-0003	•• Nut, Plain, no. 6	2
		– – – X – – –	
11	No number	•• Rear Panel and Connector Housing	1
12	02640-00010	• Support	1
		(Attaching Parts)	
13	2360-0197	• Screw, Machine, ph, no. 6-32, 3/8 in.	2
14	2190-0851	• Washer, Lock, split, no. 6	2
		– – – X – – –	
15	4040-1015	• Front Bezel	1
	4040-1023	• Front Bezel (used for Option 008)	1
		(Attaching Parts)	
16	2360-0219	• Screw, Machine, ph, no. 6-32, 3/8 in.	4
17	0905-0126	• O-Ring, 0.114 ID	4
		– – – X – – –	

Table 4-1. Terminal Replaceable Parts List (Sheet 2 of 6)

FIG. & INDEX NO.	HP PART NO.	DESCRIPTION	UNITS PER ASSY.
18	02640-20007	• Rear Door	1
19	3110-0100	• Right Hinge	1
		(Attaching Parts)	
20	02640-00025	• Hinge Support	1
21	2360-0197	• Screw, Machine, ph, no.6-32, 3/8 in.	2
		– – – X – – –	
22	3110-010	• Left Hinge	1
23	02640-00025	• Hinge Support	1
		(Attaching Parts)	
24	2360-0197	• Screw, Machine, ph, no. 6-32, 3/8 in.	2
		– – – X – – –	
25	02640-60047	• ROM Assembly	1
	1818-0157	•• I.C., ROM, MOS	1
	1818-0158	•• I.C., ROM, MOS	1
	1818-0159	•• I.C., ROM, MOS	1
	1818-0160	•• I.C., ROM, MOS	1
	1818-0161	•• I.C., ROM, MOS	1
	1818-0162	•• I.C., ROM, MOS	1
26	02640-60019	• Keyboard Interface Assembly	1
27	02640-60070	• Connector Assembly (used for Accessory 13245A)	1
28	02640-60053	• PROM Character Assembly (used for Accessory 13245A) See figure 4-5	1
29	02640-60022	• Top Plane Connector Assembly (used for Accessory 13231A)	1
	02640-60012	• Top Plane Connector Assembly (standard)	1
30	02640-60006	• Display Control Assembly	1
	1816-0613	•• I.C., 64 Character ROM (used for Option 001)	1
31	*02640-60072	• General Purpose Display Timing Assembly	1
	*02640-60088	• General Purpose Display Timing Assembly	1
	0410-0647	•• Crystal, 21.06 MHz (Y1)	1
	0410-0646	•• Crystal, 17.55 MHz (Y1) (used for Option 015)	1
32	02640-60009	• Display Memory Access Assembly	1
33	02640-60024	• Display Expansion Assembly (used for Accessory 13231A)	1
	1816-0642	•• Math Character Set (used for Accessory 13231A-201)	1
	1816-0641	•• Line Drawing Set (used for Accessory 13231A-202)	1
34	02640-60008	• Processor Assembly	1
35	02640-60065	• +4K Memory Assembly	1
36	02640-60043	• 103/202 Modem Cable Assembly (used for Accessory 13232A)	1
	02640-60059	• RS232C Cable Assembly (used for Accessory 13232C)	1
	02640-60058	• 12531/12880 Interface Cable Assembly (used for Accessory 13232B	1
37	02640-60086	• Asynchronous Data Comm Assembly	1
38	13238-60001	• 9866 Cable Assembly (used for Accessories 13238A-001 and 13246A and Option 012)	1
39	02640-60031	• Terminal Duplex Register Assembly (used for Accessories 13238A and 13246A and Option 012)	1
40	02640-60021	• CTU Top Plane Assembly (not used with Option 008)	1
41	02640-60033	• CTU Interface Assembly (not used with Option 008)	1
42	02640-60085	• Motor Cable Assembly (not used with Option 008)	1
43	02640-60032	• Read/Write Assembly (not used with Option 008)	1

NOTE: *Order part no. 02640-60088 to replace part no. 02640-60072.

Table 4-1. Terminal Replaceable Parts List (Sheet 3 of 6)

FIG. & INDEX NO.	HP PART NO.	DESCRIPTION	UNITS PER ASSY.
44	02640-60075	• Backplane Assembly	1
		(Attaching Parts)	
45	2360-0197	• Screw, Machine, ph, no. 6-32, 3/8 in.	6
46	2190-0851	• Washer, Lock, split, no. 6	6
		– – – X – – –	
	9162-0061	• Mini Cartridge (not shown) (not used with Option 008)	2
47	02640-60050	• CTU Transport Assembly (not used with Option 008)	2
		(Attaching Parts)	
48	2360-0205	• Screw, Machine, ph, no. 6-32, 3/4 in.	2
49	3050-0227	• Washer, Flat, No. 6	2
50	1520-0067	• Shock Mount	2
		– – – X – – –	
	02640-40016	•• Pawl	1
	1460-1440	•• Spring, Compression	1
		– – – X – – –	
	02640-60056	•• Head Bridge Assembly	1
		(Attaching Parts)	
	0624-0314	•• Screw, Tapping, no. 6-40	3
	2190-0003	•• Washer, Lock, split, no. 4	3
		– – – X – – –	
	2140-0450	••• Indicator Lamp DS1	1
	4040-1017	••• Shield, Light	1
		– – – X – – –	
	02640-60055	•• Motor/Tachometer Assembly	1
		(Attaching Parts)	
	1460-1381	•• Extension Spring	2
		––– X –––	
	02640-60054	•• CTU Base Assembly	1
51	02644-60003	• Mainframe Shell	1
52	02640-00021	• Access Key	2
53	02640-40002	• Display Top	1
54	3110-0099	• Hinge Top	2
		(Attaching Parts)	
55	2360-0197	• Screw, Machine, flh, no. 6-32, 3/8 in.	2
		– – – X – – –	
56	02640-00034	• CRT Shield	1
		(Attaching Parts)	
57	0510-0554	• Clip Fastener	6
		– – – X – – –	
58	02640-40003	• Right Side	1
		(Attaching Parts)	
59	2360-0197	• Screw, Machine, ph, no. 6-32, 3/8 in.	3
60	2190-0918	• Washer, Lock, split, no. 6	3
61	3050-0066	• Washer, Flat, No. 6	3
		– – – X – – –	

Table 4-1. Terminal Replaceable Parts List (Sheet 4 of 6)

FIG. & INDEX NO.	HP PART NO.	DESCRIPTION	UNITS PER ASSY.
62	02640-40004	• Left Side	1
		(Attaching Parts)	
	2360-0197	• Screw, Machine, ph, no. 6-32, 3/8 in.	3
	2190-0918	• Washer, Lock, split, no. 6	3
	3050-0066	• Washer, Flat, no. 6	3
		– – – X – – –	
63	*02640-60020	• Sweep Assembly	1
	*02640-60095	• Sweep Assembly	1
	02640-60039	• Sweep Cable Assembly (not shown)	1
64	02640-60042	• CRT Cable Assembly	1
65	02640-60037	• Fan and Cable Assembly	1
		(Attaching Parts)	
66	3030-0064	• Screw, Cap, no. 6-32, 5/8 in.	4
67	2190-0918	• Washer, Lock, split, no. 6	4
		– – – X – – –	
68	02640-60084	• CRT/Yoke Assembly	1
		(Attaching Parts)	
69	2510-0107	• Screw, Machine, ph, no. 8-32, 1/2 in.	4
70	2190-0017	• Washer, Spring, no. 8	4
71	2190-0010	• Washer, Lock, ext-tooth, no. 8	1
		– – – X – – –	
	02644-60002	• Keyboard and Cable Assembly	1
72	02640-60081	•• Keyboard Cable Assembly	1
		(Attaching Parts)	
73	2360-0197	•• Screw, Machine, ph, no. 6-32, 3/8 in.	1
74	2190-0851	•• Washer, Lock, split, no. 6	1
75	3050-0100	•• Washer, Flat, no. 6	1
76	1400-0054	•• Cable Clamp	1
		– – – X – – –	
77	02644-00002	•• Keyboard Overlay	1
78	7120-4403	•• Baud Rate Overlay	1
79	02640-40008	•• Keyboard Top	1
		(Attaching Parts)	
80	2360-0205	•• Screw, Machine, ph, no. 6-32, 3/4 in.	5
81	2190-0851	•• Washer, Lock, split, no. 6	5
82	3050-0100	•• Washer, Flat, no. 6	5
		– – – X – – –	
83	02640-60018	•• Keyboard Assembly	1
84	1990-0486	••• Light Emitting Diode, red	5
	1990-0487	••• Light Emitting Diode, yellow (not used with Option 008)	1
	1990-0485	••• Light Emitting Diode, green (not used with Option 008)	1
	0370-1129	••• BAUD RATE Knob	1
	0370-2646	••• ESC Keycap	1
	0370-2260	••• 1 ! Keycap	1
	0370-2261	••• 2 " Keycap	1
	0370-2262	••• 3 # Keycap	1
	0370-2263	••• 4 $ Keycap	1

NOTE: *Order part no. 02640-60095 to replace part no. 02640-60020.

Table 4-1. Terminal Replaceable Parts List (Sheet 5 of 6)

FIG. & INDEX NO.	HP PART NO.	DESCRIPTION	UNITS PER ASSY.
	0370-2264	··· 5 % Keycap	1
	0370-2265	··· 6 & Keycap	1
	0370-2266	··· 7 ' Keycap	1
	0370-2267	··· 8 (Keycap	1
	0370-2268	··· 9) Keycap	1
	0370-2641	··· 0 Keycap	1
	0370-2648	··· – = Keycap	1
	0370-2654	··· ^ ~ Keycap	1
	0370-2651	··· \ ¦ Keycap	1
	0370-2649	··· LINE FEED Keycap	1
	0370-2637	··· CNTL Keycap	1
	0370-2286	··· Q Keycap	1
	0370-2292	··· W Keycap	1
	0370-2274	··· E Keycap	1
	0370-2287	··· R Keycap	1
	0370-2289	··· T Keycap	1
	0370-2294	··· Y Keycap	1
	0370-2290	··· U Keycap	1
	0370-2278	··· I Keycap	1
	0370-2284	··· O Keycap	1
	0370-2285	··· P Keycap	1
	0370-2655	··· @ ` Keycap	1
	0370-2653	··· [{ Keycap	1
	0370-2650	··· _ DEL Keycap	1
	0370-2647	··· LOCK Keycap	1
	0370-2270	··· A Keycap	1
	0370-2288	··· S Keycap	1
	0370-2273	··· D Keycap	1
	0370-2275	··· F Keycap	1
	0370-2276	··· G Keycap	1
	0370-2277	··· H Keycap	1
	0370-2279	··· J Keycap	1
	0370-2280	··· K Keycap	1
	0370-2281	··· L Keycap	1
	0370-2324	··· ; + Keycap	1
	0370-2325	··· : * Keycap	1
	0370-2652	···] } Keycap	1
	0370-2635	··· RETURN Keycap	1
	0370-2636	··· SHIFT Keycap	2
	0370-2295	··· Z Keycap	1
	0370-2293	··· X Keycap	1
	0370-2272	··· C Keycap	1
	0370-2291	··· V Keycap	1
	0370-2271	··· B Keycap	1
	0370-2283	··· N Keycap	1
	0370-2282	··· M Keycap	1
	0370-2296	··· , < Keycap	1
	0370-2297	··· . > Keycap	1
	0370-2298	··· / ? Keycap	1
	02640-00019	··· Space Bar Keycap	1
	0370-0620	··· 0 Keycap (Numeric Pad)	1

Table 4-1. Terminal Replaceable Parts List (Sheet 6 of 6)

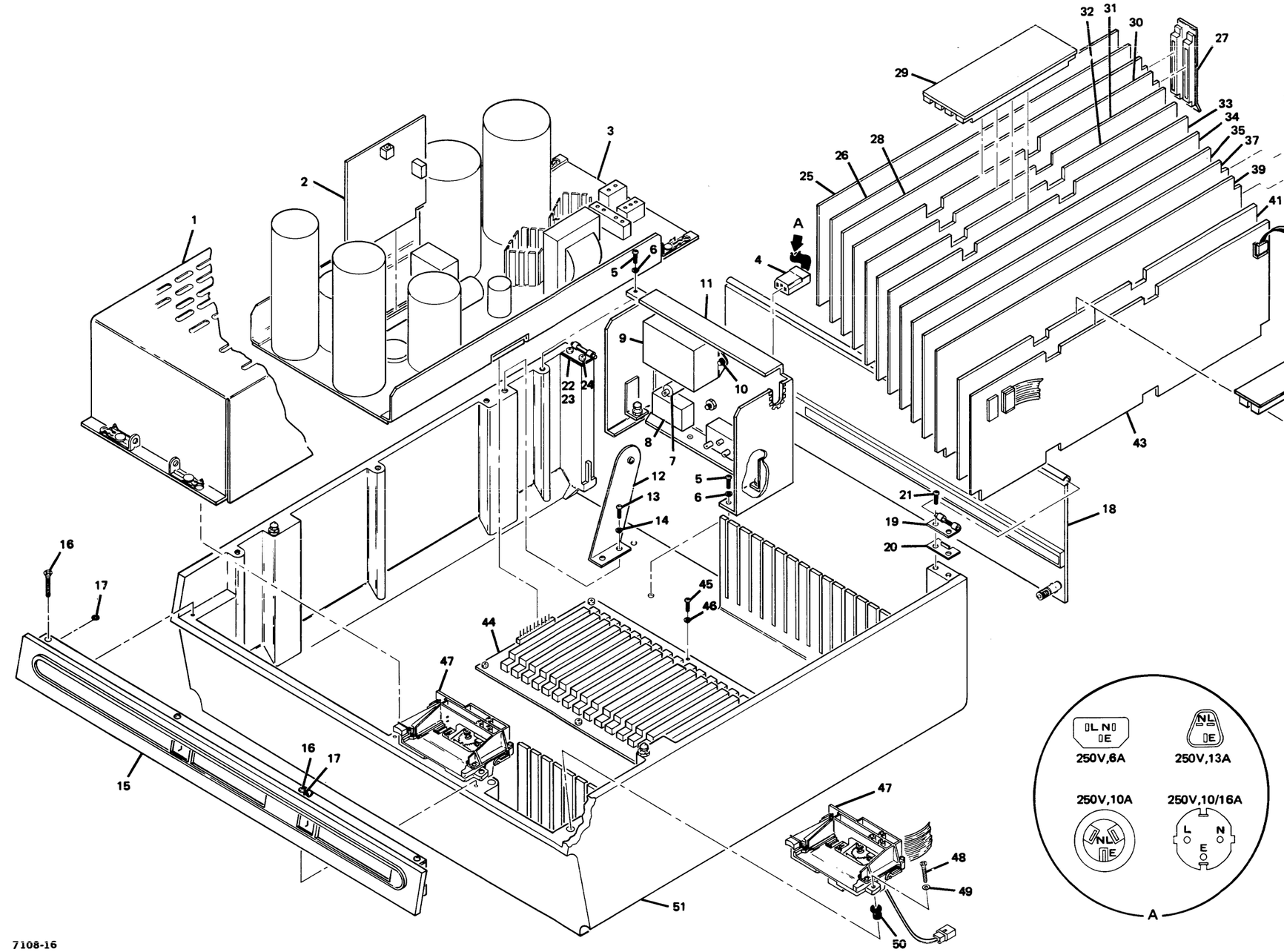
FIG. & INDEX NO.	HP PART NO.	DESCRIPTION	UNITS PER ASSY.
	0370-2312	••• 1 Keycap	1
	0370-2313	••• 2 Keycap	1
	0370-2314	••• 3 Keycap	1
	0370-2315	••• 4 Keycap	1
	0370-2316	••• 5 Keycap	1
	0370-2317	••• 6 Keycap	1
	0370-2318	••• 7 Keycap	1
	0370-2319	••• 8 Keycap	1
	0370-2320	••• 9 Keycap	1
	0370-2322	••• Keycap (Numeric Pad)	1
	0370-2656	••• CLEAR TAB Keycap	1
	0370-2657	••• SET TAB Keycap	1
	0370-2643	••• CLEAR DSPLY Keycap	1
	0370-2658	••• ROLL UP Keycap	1
	0370-2659	••• ROLL DOWN Keycap	1
	0370-2638	••• NEXT PAGE Keycap	1
	0370-2639	••• PREV PAGE Keycap	1
	0370-2879	••• ↖ (Home) Keycap	1
	0370-2640	••• Arrow Keycap	4
	0370-2644	••• Operating Function Keycap	15
	0370-2765	••• f_1 Keycap	1
	0370-2766	••• f_2 Keycap	1
	0370-2767	••• f_3 Keycap	1
	0370-2768	••• f_4 Keycap	1
	0370-2769	••• f_5 Keycap	1
	0370-2770	••• f_6 Keycap	1
	0370-2771	••• f_7 Keycap	1
	0370-2772	••• f_8 Keycap	1
	0362-0017	••• Function Keycap, Read and Record (not used with Option 008)	2
	0370-2877	••• Backspace Keycap	1
	0370-2878	••• TAB Keycap	1
	0370-2898	••• Olive Black Keycap	1
	0370-2894	••• Green Keycap (not used with Option 008)	1
	0370-2895	••• Yellow Keycap (not used with Option 008)	1
85	9160-0233	•• Loudspeaker Assembly	1
		(Attaching Parts)	
86	2360-0117	•• Screw, Machine, ph, no. 6-32, 3/8 in.	2
87	1400-0054	•• Mounting Clamp	2
		– – – X – – –	
88	0403-0324	•• Rubber Bumper	4
89	02640-40007	•• Keyboard Bottom	1
	8570-0585	•• Keycap Removal Tool (not shown)	1
	9866A	Printer (not shown) Used for Accessory 13246A and Option 012	1
	9300-0468	Cleaning Swab (not shown)	10
	8500-1251	Cleaning Solvent (not shown)	1

Table 4-2. PROM Character PCA Replaceable Parts List

REFERENCE DESIGNATION	HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.
C1, 2	0180-0393	C: Fxd Ta 39 μF ±10%, 10 VDCW	56289	150D396X9010B2-DYS
C3 thru C16	0160-2055	C: Fxd Cer 0.01 μF +80 -20%, 100 VDCW	56289	C023F101F103ZS22-CDH
R1, 2	1810-0121	R: Fxd network 8 x 1K ohms 5%	56289	200C-1855-CRR
U6, 16	1820-1245	IC: TTL Quad 2-inpt AND gate	01245	SN74LS155N
U7, 9	1820-1208	IC: TTL Quad 2-inpt OR gate	01245	SN74LS32N
U8	1820-1244	IC: TTL 4-inpt multiplexer	01245	SN74LS153N
U10, 7, 19	1820-1246	IC: TTL Quad 2-inpt AND gate, open collector	01245	SN74LS09N
U18	1820-1144	IC: TTL Quad 2-inpt NOR gate	01245	SN74LS02N
XU1 thru XU5, XU11 thru XU15	1200-0541	Socket, IC, 24-pin	09922	DILB24P-1

Table 4-3. Code List of Manufacturers

CODE NO.	MANUFACTURER	ADDRESS
01245	Texas Instruments, Inc., Component Group	Dallas, Texas
09922	Burndy Corp.	Norwalk, Conn.
56289	Sprague Electric Co.	North Adams, Mass.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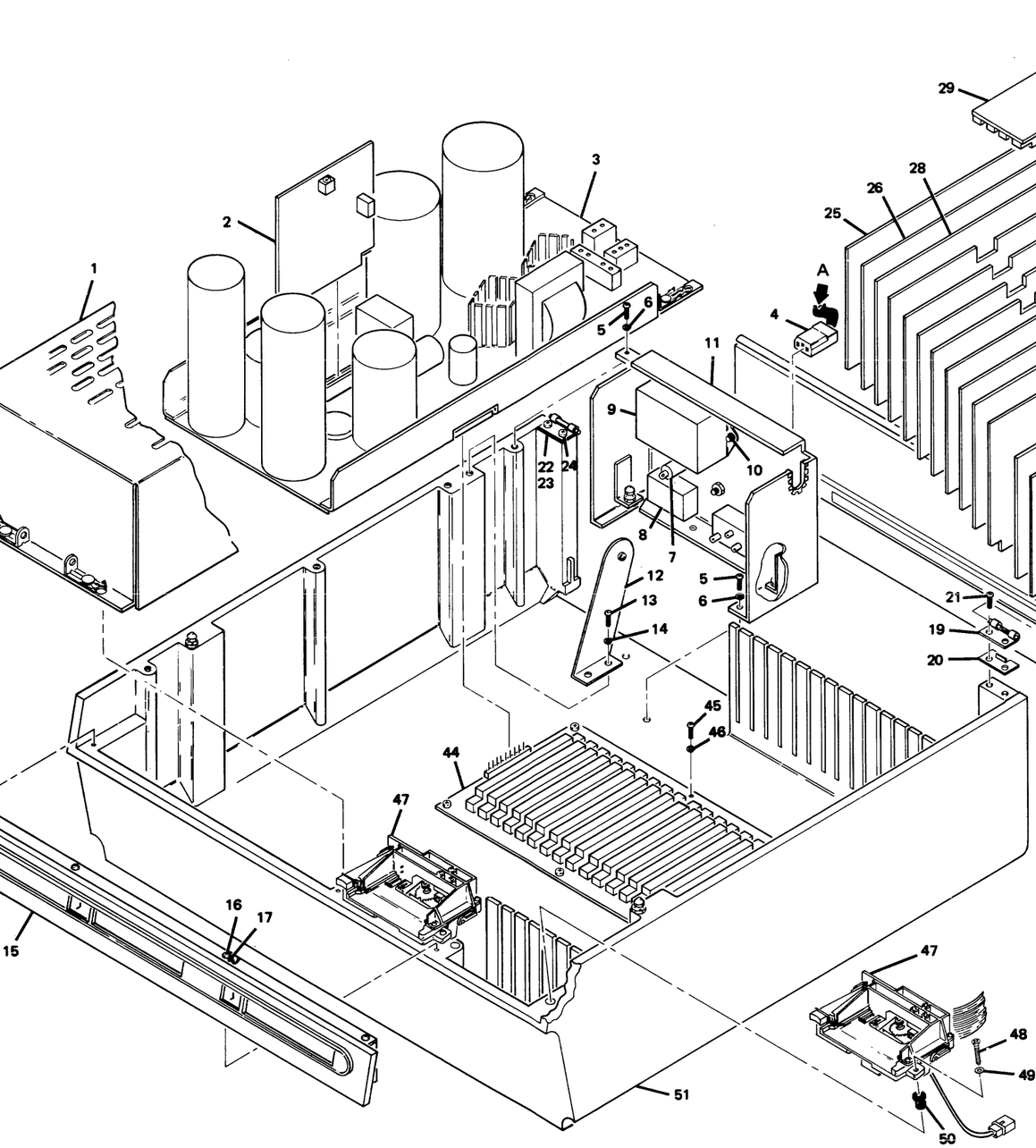
A
250V,6A
250V,13A
250V,10A
250V,10/16A
L
N
E

7108-16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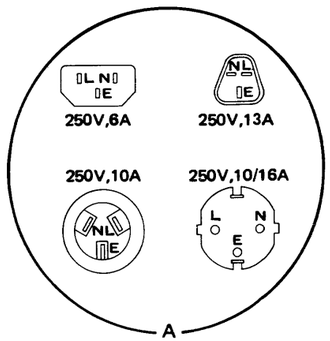
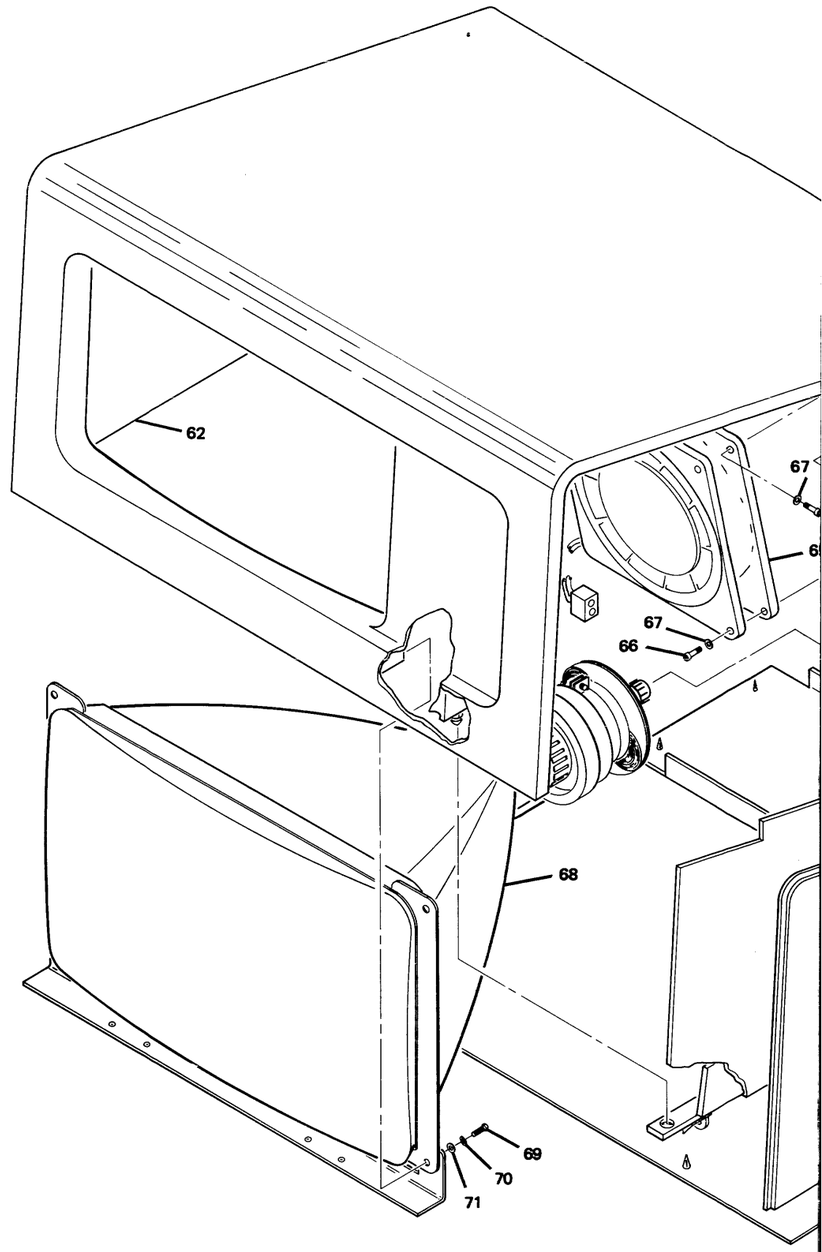
A


L N
E
250V,6A
250V,13A
250V,10A
250V,10/16A
L
N
E
A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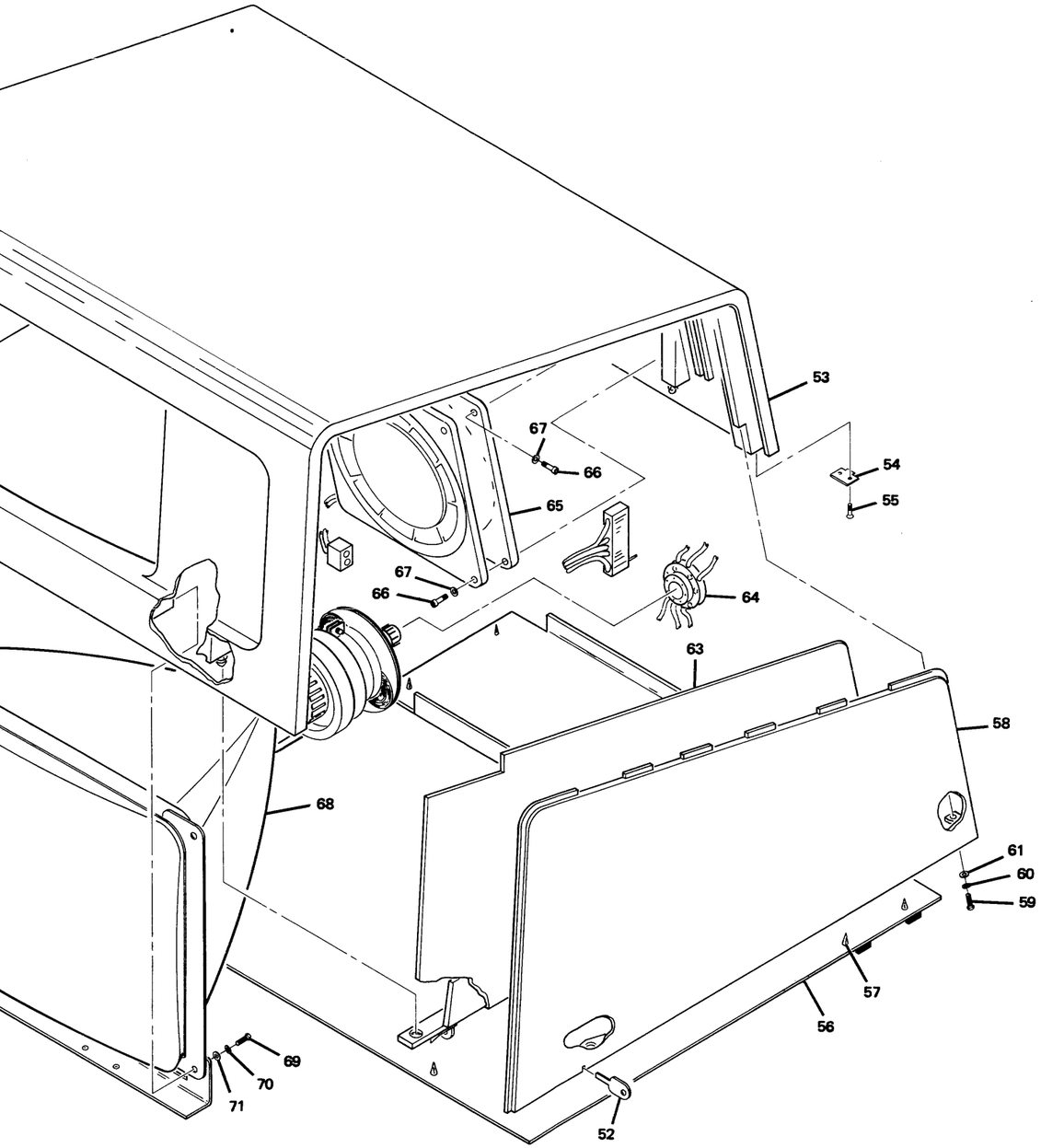


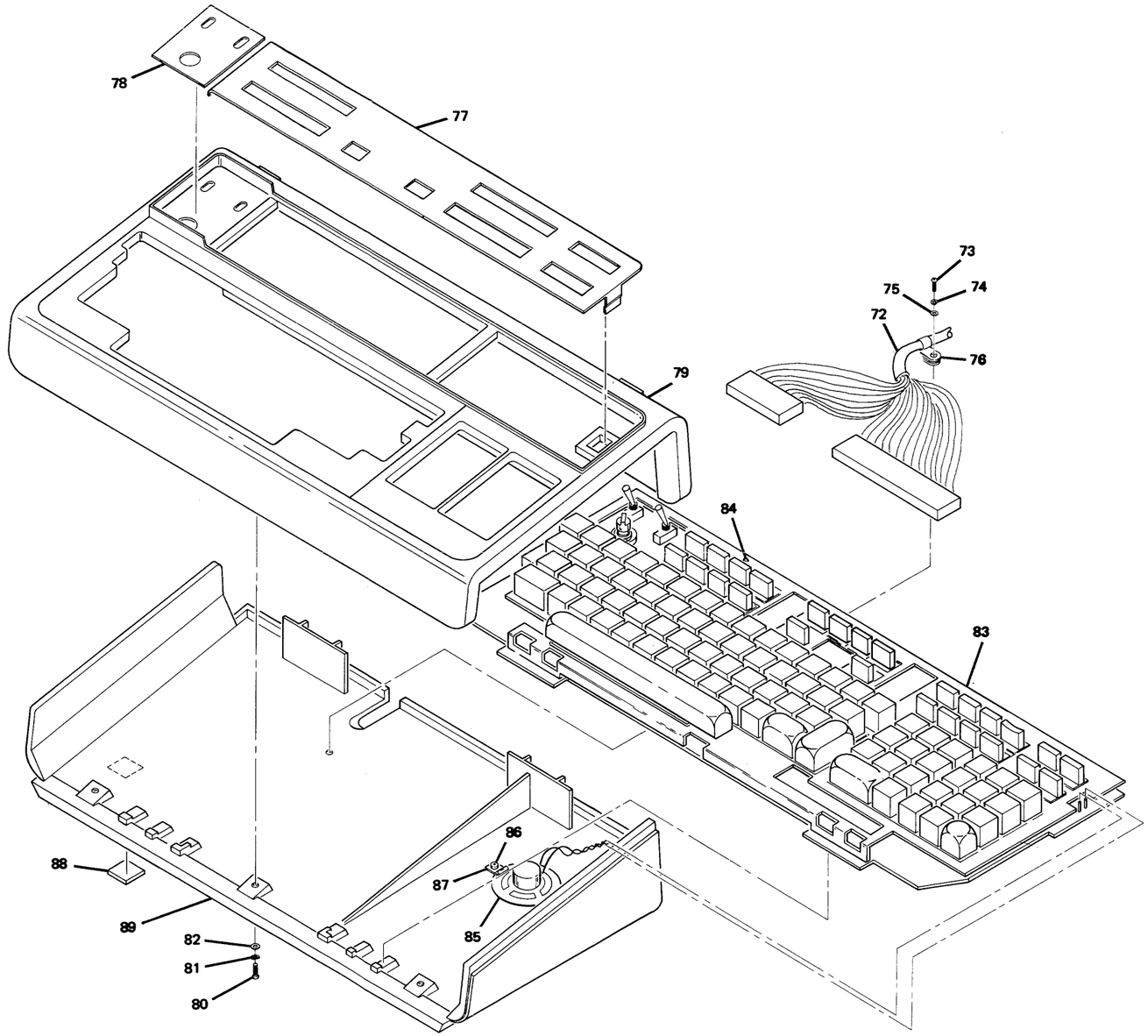
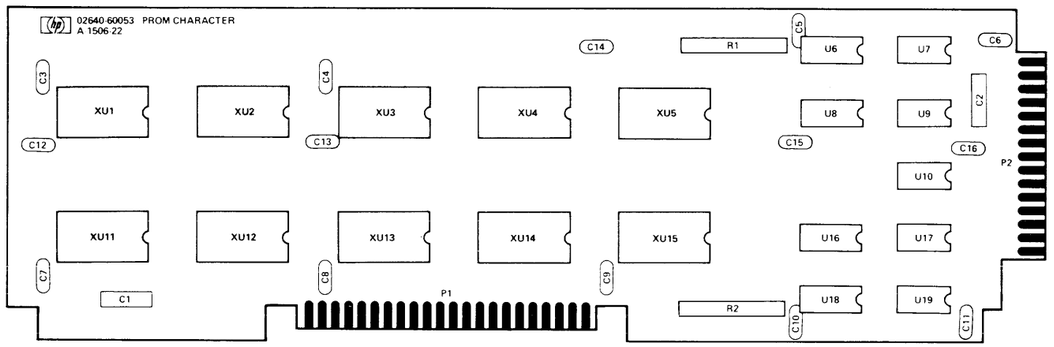
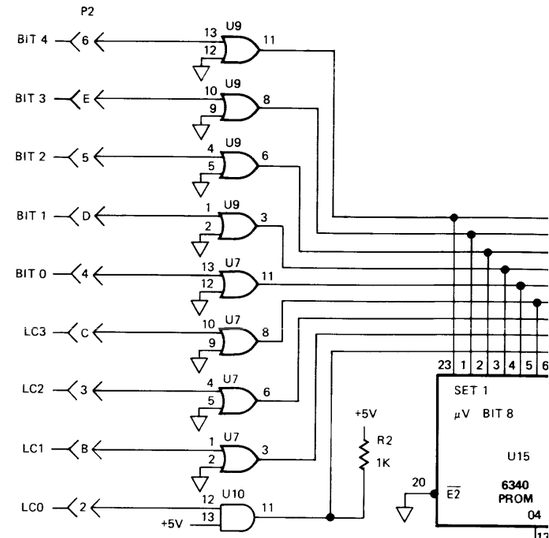
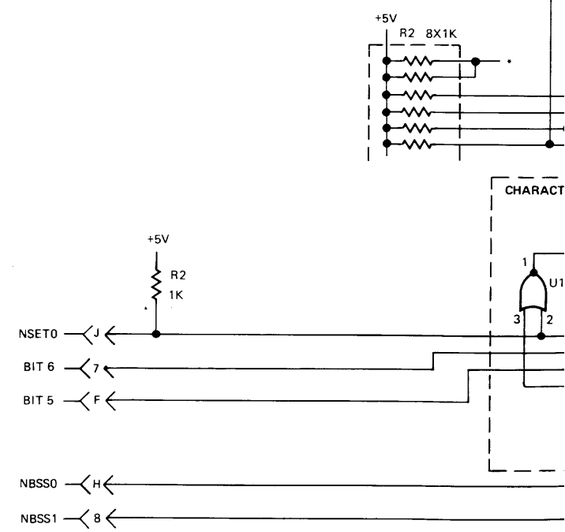


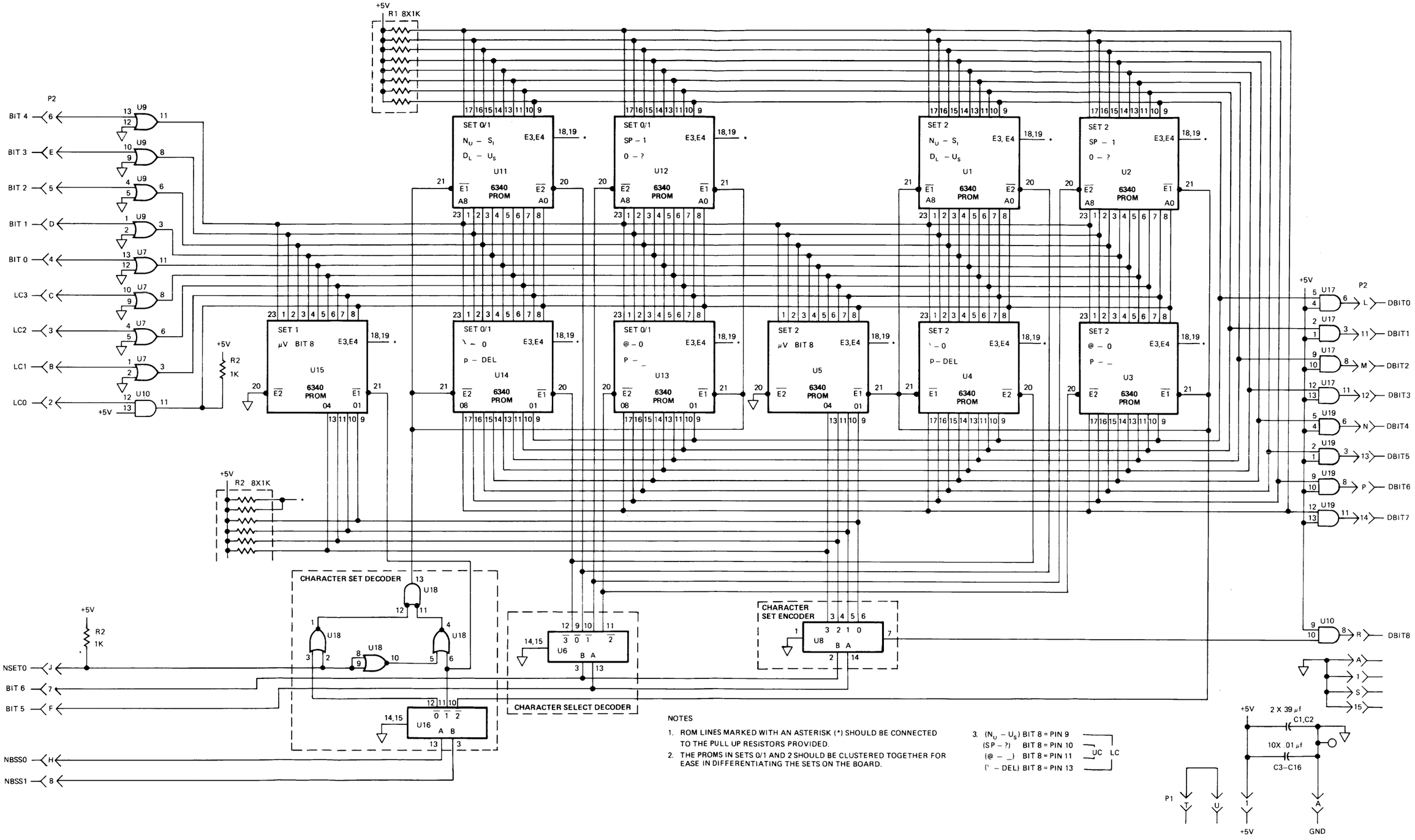
Figure 4-4. HP 2644A Terminal, Exploded View


02640-60053 PROM CHARACTER
A 1506-22
XU1
XU2
XU3
XU4
XU5
XU11
XU12
XU13
XU14
XU15
U6
U7
U8
U9
U10
U16
U17
U18
U19
R1
R2
C1
C2
C3
C4
C5
C6
C7
C8
C9
C10
C11
C12
C13
C14
C15
C16
P1
P2


P2
BIT 4
BIT 3
BIT 2
BIT 1
BIT 0
LC3
LC2
LC1
LC0
U9
U7
U10
+5V
R2
1K
SET 1
μV BIT 8
U15
6340
PROM
04
E2


+5V
R2 8X1K
CHARACT
+5V
R2
1K
NSET0
BIT 6
BIT 5
NBSS0
NBSS1
U1

7077-25



NOTES

1. ROM LINES MARKED WITH AN ASTERISK (*) SHOULD BE CONNECTED TO THE PULL UP RESISTORS PROVIDED.
2. THE PROMS IN SETS 0/1 AND 2 SHOULD BE CLUSTERED TOGETHER FOR EASE IN DIFFERENTIATING THE SETS ON THE BOARD.
3. $(N_U - U_S)$ BIT 8 = PIN 9
   (SP – ?) BIT 8 = PIN 10
   (@ – _) BIT 8 = PIN 11
   (\ – DEL) BIT 8 = PIN 13
   UC LC

7077-25

Figure 4-5. PROM Character PCA, Schematic Diagram

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